Fabrication and Characterization of Suspended Uniaxial Tensile Strained-Si Nanowires for Gate-All-Around n-MOSFETs

P. Hashemi^a, M. Canonico^b, J.K.W. Yang^c, L. Gomez^a, K.K. Berggren^c, and J. L. Hoyt^a

^a MIT Microsystems Technology Laboratories, Cambridge, MA 02139, USA
^b Physical Analysis Laboratory, Freescale Semiconductor Inc., Tempe, AZ, USA
^c MIT Nano Structures Laboratory, Cambridge, MA 02139, USA

Suspended strained-Si nano-wires (NWs) were fabricated from a highly biaxially strained-Si substrate (with an initial stress of 2.16 GPa). Using e-beam lithography, ~25nm thick NWs with the widths in the range of 20 to 80 nm were fabricated and the stress was investigated by UV micro-Raman spectroscopy. Suspended NWs are strained to an average uniaxial tensile stress level of ~2.1 GPa which is almost independent of NW width, in the range studied in this work. Ultra-dense (25 NWs per micron) sub-20 nm suspended strained-Si NWs were fabricated using resolutionenhanced lithography to improve the Raman signal-to-noise ratio. A tensile in-plane stress level of 1.7GPa was measured for 18 nmwide NWs at 40 nm pitch. Gate-all-around n-MOSFETs were these fabricated based on strained-Si NWs. Electrical measurements on these MOSFETs demonstrate near ideal subthreshold behavior, very high on-to-off ratio and current drive and transconductance enhancement of ~2X over unstrained NWs.

Introduction

Non-planar, multi-gate, and Gate-All-Around (GAA) nanowire (NW) MOSFET architectures are promising candidates for deeply-scaled CMOS technology due to their excellent electrostatic control and immunity to short-channel effects (1-3). Application of high levels of strain to these structures has the potential to significantly enhance the carrier mobility and velocity. For planar n-MOSFET operation, uniaxial tension in <110> direction has been demonstrated to have the optimum performance among candidate strain and orientations. Unlike biaxial tension, the relative change in electron mobility obtained for uniaxial tension is directly correlated to relative change in ballistic velocity (4). This is attributed to the reduction in the conductivity effective mass in addition to the band splitting in the conduction band minima (5). There are very few reports applying strain to NWs. In previous work, strain was induced by bending the NWs using thermal oxidation (6) or metal stressors (7). However, due to the bending of nanowires, these techniques are not practical for CMOS integration. One possible approach to create uniaxial tensile substrates is to elastically relax biaxially strained-Si in one direction by etching (8, 9). This method has recently been utilized to fabricate strained-Si tri-gate MOSFETs with enhanced performance (10). There are no reports on application of this method to free standing NWs. In this paper, top-down fabrication of ultra-dense suspended uniaxially tensile strained-Si NWs suitable for GAA n-MOSFETs is demonstrated. The suspended architecture improves the device effective width in a given chip area and the corresponding current drive, compared to planar, or tri-gate

devices with the same channel/wire width. In addition, the tensile strained NWs are straight and do not suffer from bending issues. The stress levels in this study are larger than previous reported data on tri-gate structures (10). In the following sections, the dependence of stress on NW width is investigated. In the last section, the performance enhancement of GAA n-MOSFETs based on these strained-Si NWs is discussed.



Fig. 1: Schematic process flow of modified bond and etch-back technique to fabricate biaxial 30% SSDOI (y=0.3 and 0 < x < y).

Substrate and Strained-Si NW Fabrication

Starting wafers were 6" Strained-Si Directly on Insulator (SSDOI), strained to a virtual Si_{0.70}Ge_{0.3} substrate. A modified bond and etch-back technique was used to create 30% SSDOI substrates (11, 12). The process flow is shown in Fig. 1. Note there is no SiGe in the final structure. A heterostructure stack of strained-Si (30nm)/relaxed Si_{0.70}Ge_{0.3} (100nm)/ strained-Si (11nm)/relaxed Si_{0.70}Ge_{0.3} (500nm)/ Si_{1-x}Ge_x graded buffer layer (1.5µm, 0<x<0.3) was epitaxially grown on p- Si substrate followed by deposition of ~270 nm Low-Pressure Chemical Vapor Deposition (LPCVD) SiO₂. All epitaxial layers were grown in an Applied Material Epi CenturaTM reactor. The wafers were then bonded to a handle wafer coated with 100 nm thermally grown oxide for 2 hours at a temperature of 600°C (Fig. 1(a)). A 1.5 µm-thick protective PECVD oxide was deposited on the backside of the handle wafers to protect the substrate while etching the Si and SiGe graded buffer layer. The substrates were then ground, polished and etched to remove SiGe/strained-Si/SiGe (Fig. 1(b), (c)). The strained-Si was thinned to ~25nm by chemical oxidation and removal. Final strained Si layer thickness was measured by a SIMS/TEM calibrated UV laser interferometer.

The fabrication process of strained-Si NWs is schematically shown in Fig. 2. A ~90nm 4% hydrogen silsesquioxane (HSQ) XR-1541 negative tone e-beam resist (from Dow Corning[™]) was spun on the substrate (3000 rpm, 1 minute) and prebaked at 80°C for 4 minutes (Fig. 2(a)). E-beam exposure was performed in a Raith150[™] scanning e-beam lithography system at an acceleration voltage of 30keV and a dose of 1.2mC/cm².

The smallest available electron beam size of 2 nm was chosen to minimize the line edge roughness. Multiple parallel NWs (8-10 wires) ending on two pads were exposed. The width of the wires was in the range of 20 to 80 nm. The NWs were 2 μ m long and the pads are 2 μ m × 1 μ m rectangles. The pitch size (distance between NW centerlines) was 100 nm for 20, 25, 30, and 35 nm-wide nanowires and 120, 150, 180, and 200 nm for 40, 50, 60 and 80 nm-wide NWs, respectively. The dose and pitch were optimized to minimize proximity effects. High NW density is an important parameter to obtain a measurable Raman signal. The resist was developed in 25% TMAH for 1 minute at the room temperature followed by a rinse and dry step. The Si was dry etched by Cl₂/Ar in a reactive ion etcher (Fig. 2(b)). The NWs were suspended by partial etching of the buried oxide (80 to 100 nm removed) in 100:1 HF solution.



Fig. 2: Schematic process flow of suspended strained-Si NWs: (a) after spinning ~90nm e-beam resist, (b) after resist development and strained-Si RIE, (c) after nanowire suspension in dilute HF, and (d) top-down view.



Fig. 3: (a) SEM image of a strained-Si NW with e-beam resist on top, (b) line edge profile of part (a) showing an average of 20 nm with $3\sigma_{avg} = 2.4$ nm, (c) tilted SEM image of 20 nm-wide NWs before resist removal and (d) tilted SEM image of 25nm-wide suspended strained-Si NWs.

A schematic cross section and top view of suspended strained-Si NW fabrication is shown in Fig. 2(c) and Fig. 2(d), respectively. The width of NWs after suspension was measured by scanning electron microscopy (SEM) and found to be as expected. Fig. 3(a) shows a strained-Si NW line with resist on top. The NW's edge profile is shown in Fig. 3(b). Based on this profile, the line has an average width of 20 nm with $3\sigma_{avg} = 2.4$ nm. The tilted SEM image of the 20nm-wide wires and pads (with resist on top) is shown in Fig. 3(c). Fig. 3(d) shows the tilted SEM micrograph of 25nm-wide NWs after suspension.

Stress Characterization of Suspended Strained-Si NWs

UV Micro-Raman spectroscopy was used to analyze the level of stress in the suspended strained-Si NW and pad regions (13, 14). The UV spectrometer was operated in additive mode using 325 nm He-Cd laser line. The UV laser power density was $\sim 300 \text{kW/cm}^2$ and the beam diameter was $\sim 0.4 \mu\text{m}$. Fig. 4 shows the Raman spectra of the Si LO phonon from a 40 $\mu\text{m} \times 40 \mu\text{m}$ patterned square region, which approximates the original blanket SSDOI layer strain. The Raman spectrum of a bulk Si wafer is also shown for comparison. The Si LO phonon frequency is observed to be red-shifted by -8.9 cm⁻¹, equivalent to 2.16GPa biaxial stress. The measured stress is consistent with the nominal value of 30 at. % Ge (\pm 1 at. % Ge) in the relaxed SiGe donor substrate.



Fig. 4: Raman spectra of the Si LO phonon from unstrained bulk Si (dashed line) and the 40 µm square box (solid line). The measured Si peak shift is consistent with the strain expected in Si grown on a relaxed SiGe donor substrate with 30% Ge concentration.

The Raman spectra of the Si-Si LO phonon mode of suspended strained-Si NWs with pads attached to the buried oxide with widths of 40, 30, 25, and 20 nm are shown in Fig. 5(a)-(d), respectively. The NWs were ~25 nm thick and 2 μ m long. The laser was scanned from pad to pad in a direction parallel to the NW length, as schematically shown in the inset of Fig. 5(a). For the Raman spectra of the 40 nm-wide NWs (Fig. 4(a)), spectra #18-20 correspond to the Si substrate and spectrum #22 begins to show an asymmetry on the low energy side. The broadening arises due to simultaneous

illumination of the SSOI pad and substrate. In spectra #23, #24 and #25, the Si LO frequency further redshifts to ~515 cm⁻¹ and the Si substrate intensity diminishes as the laser beam scans across the pad. Beginning with spectrum #26, the frequency blueshifts slightly to ~516 cm⁻¹ and the substrate signal reappears as the laser beam transitions onto the wires and off of the pad. The increasing substrate intensity at ~520 cm⁻¹ results from the laser beam passing between the wires. Starting with spectrum #32, the strained Si signal intensity increases and the substrate intensity decreases as the laser beam begins transitioning from the wires back onto the second pad. Spectra #33 and #34 are representative of the pad alone. At spectrum #35 and #36 the laser beam is beginning to move from the pad back onto the substrate, and thus the overall signal is a convolution of both strained Si and substrate frequencies. Finally, spectra #37 and #38 represent a signal collected solely from the substrate.



Fig. 5: Raman spectra of the Si-Si LO phonon mode as the laser is scanned from pad to pad in a direction parallel to the NW length, as shown in the inset of (a), for (a) 40 nm, (b) 30 nm, (c) 25 nm, and (d) 20 nm-wide NWs. The NWs are \sim 25 nm thick and 2 µm long.



Fig. 6: Total in-plane stress extracted from the data assuming biaxial isotropic strain for each spectrum along the Raman line scan for NWs with widths of (a) 40, (b) 30, (c) 25, and (d) 20 nm.

All strain calculations are based on a manual software fit to the spectral data using one or two Lorentzian functions depending on the overall signal line shape and position of the laser beam, after canceling the linear background signal (for example of such a fit, see Fig. 9). Stress errors were calculated based on various sources such as unstrained Si reference frequency, SSOI frequency, phonon deformation potentials, and elastic constants. These measurements were performed at the limit of both the spatial and spectral resolution of convention UV micro-Raman and the data and analysis should be viewed within that context. Additionally, micro-Raman configurations are not conducive to observing the TO phonon band and thus a planar stress model with biaxial strain is generally assumed. Therefore, to calculate stress in NW and pad regions from the observed peak shifts, isotropic biaxial relaxation was assumed. The total in-plane stress, $\sigma_{xx} + \sigma_{yy}$, for the structures with NW widths of 40 to 20 nm are shown in Fig. 6(a)-(d). The location of the spectra corresponding to the signal from the NWs is indicated in each plot. It should be noted that the y-axis in Fig. 6 corresponds to the sum of the stress in two perpendicular in-plane directions, and micro-Raman measurements are not able to resolve the individual in-plane stress components. Typically for large features or blanket films which are strained due to lattice mismatched epitaxial growth, the planar stress model is used. However, for small patterned features with relatively high aspect ratios, uniaxial relaxation can occur (8-10). We believe that the biaxial to highly asymmetric strain (close to uniaxial) transition occurred upon patterning the SSDOI films (16). After suspension, since the wires are free standing, elastic in-plane relaxation in the direction perpendicular to the NWs is highly likely, and we can assume that the strain is mainly uniaxial with only a longitudinal component remaining. Mechanical stress simulations similar to those in (16) are consistent with this interpretation.

The total in-plane stress at the center of the NW region as a function of NW width is plotted in Fig. 7 (left axis). As can be seen from this plot, the NWs are strained to a total in-plane stress of ~2.1GPa with minimal width dependence. The right-hand axis corresponds to the associated Raman signal to noise ratio (SNR). Note that the signal to noise ratio falls significantly as the NW width is decreased. This is mainly due to fact that nanowire fill factor is decreased below 40 nm. NWs with widths of less than 40nm were fabricated at a constant pitch size of 100 nm. As the gap size is increased by reducing the NW width, the signal obtained from the substrate increases. Therefore, it is more difficult to deconvolve the signals from the wires and SNR is reduced.



Fig. 7: Total in-plane stress (circles, left axis) and corresponding signal-to-noise ratio (squares, right axis) for spectra collected from the NWs midway between the two pads. The NWs are \sim 25 nm thick and 2 µm long.

Fabrication and Characterization of Ultra-Dense Suspended Strained-Si NWs

In an attempt to improve the Raman signal-to-noise ratio for nanowires with dimensions around 20 nm or less, ultra dense suspended strained-Si NWs were fabricated utilizing resolution improved e-beam lithography. 6% XR1541[™] negative tone e-beam resist was first diluted in Methyl Iso-Butyl Ketone (MIBK) in a 1 HSQ: 3 MIBK by volume ratio and spin-coated onto the sample at a speed of 6000 rpm to a thickness of 35 nm. The sample was then exposed in a Raith150[™] electron-beam lithography tool at a 30 kV acceleration voltage. NW structures were exposed using single-pass lines with the dose of 14.0-24.3 mC/cm while the large pads were exposed as filled-in rectangles using a dose of 2.2 mC/cm². The sample was typically exposed within 4 hours of resist spincoating. A high-contrast salty development process of HSQ was used to achieve dense, high-resolution structures (17). The sample was then developed in an aqueous mixture of 1% NaOH and 4% NaCl at 24C for 4 mins, then rinsed in de-ionized (DI) water and dried using a pressurized N_2 gun. The addition of NaCl salt to aqueous NaOH developer was found to increase the contrast of the resist, which enabled the fabrication of highresolution nanostructures with minimal loss in resist thickness (17). The subsequent process steps were similar to the steps used to fabricate moderately dense NWs. Sample high-resolution SEM images of 10 nm resist lines in 30 nm pitch are shown in Fig. 8(a). Fig. 8(b) shows a tilted SEM image of 18nm-wide ultra-dense suspended strained-Si NWs. These NWs are ~ 25 nm thick and 2 μ m long. Inset shows the plan-view SEM image of these NWs. The density of the NWs is 25 NW/µm.



Fig. 8: (a) High-resolution SEM image of ultra dense 10 nm-wide resist lines in 30 nm pitch using high-contrast e-beam lithography; (b) SEM image of ultra-dense 18 nm-wide suspended strained-Si NWs. The NWs are \sim 25 nm thick and 2 µm long and the pitch is 40 nm.

UV micro Raman spectroscopy with a 325 nm He-Cd laser line was used to measure the stress in ultra-dense suspended NWs. The Raman spectrometer was operated at a high power density of 280kW/cm² to enhance the relatively weak SNR from the NWs. Fig. 9 shows the spectra of the Si LO phonon for NWs measured at power densities of 122 and 280 kW/cm². The total in-plane stress measured at higher power density is around 0.18 GPa more than the stress measured at lower power density. This artificial shift in the phonon frequency is due to laser heating, which hydrostatically expands the lattice and redshifts the phonon frequency (15).



Fig. 9: Low (a) and high (b) laser power spectra of the Si LO phonons from the NWs and substrate. Thermal expansion contributes to an apparent ~ 0.18 GPa total in-plane stress shift in the high power case.

Raman spectra of the Si-Si LO phonon mode and total in-plane stress for ultra dense 18 nm-wide NWs at 40 nm pitch are shown in Fig. 10 (a) and (b), respectively. The Raman spectra associated with the pads and 1 μ m long NWs are indicated. The NWs are strained to total in-plane stress of 1.7 GPa, which is slightly lower than the value obtained in the previous section for the 20 nm-wide NWs.



Fig. 10: (a) Raman spectra of the Si-Si LO phonon mode and (b) total in-plane stress as the laser is scanned from pad to pad in a direction parallel to the NW length, for ultra dense 18nm-wide NWs. The nanowire pitch size was reduced to 40 nm to improve the Raman signal-to-noise ratio.

Electrical Characteristics of GAA strained-Si n-MOSFETs

GAA n-MOSFETs were fabricated based on these suspended strained-Si NWs (18). Starting from ~20nm-thick substrates, the nanowires were thinned to ~10-13nm during processing prior to gate stack deposition. The nanowires were coated with low-temperature oxide (LTO) and ~80 nm *in-situ* N+ doped poly-Si, wrapping all around the NWs. The subsequent process was similar to the fabrication process of planar thin-body SSDOI (19). For comparison, similar unstrained-Si substrates went through the same fabrication process.

Fig. 11(a) shows the transfer characteristics of GAA strained-Si and unstrained-Si NW n-MOSFETs. Each transistor consists of 10 parallel NWs. The current was scaled to the number of NWs. The wires are \sim 30nm wide, \sim 10-13nm thick and \sim 1µm long. The devices display near ideal subthreshold slope of \sim 65mV/dec at room temperature, with large on-to-off ratio. The 0.11mV shift in the threshold voltage is consistent with the uniaxial strain in NWs (20). The low field extrinsic transconductance of these devices is shown in Fig. 11 (b). Assuming the same device dimensions, the strained-Si NWs show an enhancement slightly exceeding 2X, in maximum transconductance and current drive current (at a given gate overdrive) compared to unstrained-Si NWs. The enhancement degrades at higher gate voltages due to the larger contribution of series resistance.



Fig. 11: (a) Transfer characteristics and (b) extrinsic transconductance of GAA unstrained-Si and strained-Si NW n-MOSFETs. NWs are ~13nm thick, ~30nm wide and 1 μ m long with ~13nm LTO/~80nm N⁺ poly-Si gate stack.

Summary and Conclusion

In summary, the fabrication of suspended strained-Si nanowires suitable for gate-allaround n-MOSFETs has been demonstrated. Starting substrates were highly biaxial strained Si directly-on-insulator (strain $\sim 1.2\%$) with a thickness of 20 to 25 nm. Free standing nanowires with dimensions of 20 to 80 nm were fabricated using e-beam lithography, RIE, and wet etching process. Nanowire stress was comprehensively analyzed by UV micro-Raman spectroscopy. The results indicate that suspended nanowires are strained to an average stress level of 2.1GPa which is almost width independent in the range of study. In an attempt to decrease the wire dimensions as well as to improve the Raman signal-to-noise ratio, ultra-dense NWs, with the pitch size as small as 40 nm, were successfully fabricated and their stress was also measured by micro-Raman spectroscopy. The effect of heating of the wires by a higher laser power was also investigated. A total in-plane stress level of 1.7 GPa was measured for ultra-dense 18 nm-wide nanowires. N-channel MOSFETs with Gate-all-around architecture were fabricated using the strained Si nanowire process. The devices show near ideal subthreshold slope and very high on-to-off ratio ($\sim 10^8$). The strained nature of these NWs was electrically confirmed by the threshold voltage shift, and drive current and transconductance enhancement (at a given gate overdrive) compared to unstrained Si NW MOSFETs.

Acknowledgments

The authors acknowledge the support of the FCRP MSD Center. The authors would like to thank G. Riggott, M. K. Mondol, M. Kim and staff and colleagues in the Microsystems Technology Laboratories and SEBL/RLE at MIT. We would also like to thank A. Khakifirooz and D. A. Antoniadis for helpful discussions.

References

- 1. S-D Suk et al., Technical Digest International Electron Devices Meeting, 717 (2005).
- N. Singh, A. Agarwal, L. K. Bera, T. Y. Liow, R. Yang, S. C. Rustagi, C. H. Tung, R. Kumar, G. Q. Lo, N. Balasubramanian, and D. L. Kwong, *IEEE Electron Device Lett.*, 27, 383 (2006).
- O. Gunawan, L. Sekaric, A. Majumdar, M. Rooks, J. Appenzeller, J. W. Sleight, S. Guha, and W. Haensch, *Nano Lett.*, 8, (2008).
- 4. A. Khakifirooz and D. A. Antoniadis, *Technical Digest International Electron Devices Meeting*, 667 (2006).
- 5. K. Uchida, T. Krishnamohan, K.C. Saraswat, and Y. Nishi, *Technical Digest International Electron Devices Meeting*, 129 (2005).
- K. E. Moselund, P. Dobrosz, S. Olsen, V. Pott, L. De Michielis, D. Tsamados, D. Bouvet, A. O'Neill and A. M. Ionescu, *Technical Digest - International Electron Devices Meeting*, 191 (2007).
- N. Singh, W. W. Fang, S. C. Rustagi, K. D. Budharaju, Selin H. G. Teo, S. Mohanraj, G. Q. Lo, N. Balasubramanian, and D.-L. Kwong, *IEEE Electron Device Lett.*, 28, 558 (2007).
- 8. R.Z. Lei, W. Tsai, I. Aberg, T.B. O'Reilly, J.L. Hoyt, D.A. Antoniadis, H.I. Smith, A.J. Paul, M.L. Green, J. Li, and R. Hull, *Appl. Phys. Lett.*, **87**, 251926 (2005).
- 9. K. Usuda, T. Irisawa, T. Numata, N. Hirashita, and S. Takagi, *Semicond. Sci. Technol.*, **22**, S227 (2006).

- 10. T. Irisawa, T. Numata, T. Tezuka, N. Sugiyama, and S.-I. Takagi, *Technical Digest International Electron Devices Meeting*, 147 (2006).
- 11. T.S. Drake, C.N. Chleirigh, M.L. Lee, A. J. Pitera, E.A. Fitzgerald, D.A. Antoniadis, D.H. Anjum, J. Li, R. Hull, N. Klymko, and J.L. Hoyt, *Journal of Electronic Materials*, **32**, 972 (2003).
- 12. I. Åberg, O. O. Olubuyide, C. Ní Chléirigh, I. Lauer, D. A. Antoniadis, J. Li, R. Hull, and J. L. Hoyt, *Technical Digest VLSI Symp.*, 52 (2004)
- 13. P. Dobrosz, S. J. Bull, S. H. Olsen, and A. G. O'Neill, *Surf. Coat. Technol.*, **200**, 1755 (2005).
- 14. V. Vartanian et al., IEEE Trans. Semicond. Manuf., 4, 381 (2006).
- 15. T. R. Hart, R. L. Aggarwal, and Benjamin Lax, Phys. Rev. B, 1, 638 (1970).
- 16. P. Hashemi, L. Gomez, M. Canonico, M. D. Robertson and J. L. Hoyt, *Appl. Phys. Lett.*, **91**, 083109 (2007).
- 17. J. K. W. Yang and K. K. Berggren, J. Vac. Sci. Technol. B, 25, 2025 (2007).
- 18. P. Hashemi, L. Gomez, M. Canonico, and J. L. Hoyt, *Technical Digest Device Research Conf.* (2008).
- 19. L. Gomez, I. Åberg and J. L. Hoyt, *Electron. Device Lett.*, 28, 285 (2007).
- 20. T. Irisawa, T. Numata, T. Tezuka, K. Usuda, N. Sugiyama, and S-I. Takagi, IEEE Trans. Electron Devices, **55**, 649 (2008).