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Suppressed Critical Current in Superconducting Nanowire Single-Photon Detectors With High Fill-Factors

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Abstract—In this work we present a new fabrication process that enabled the fabrication of superconducting nanowire single photon detectors SNSPD with fill-factors as high as 88% with gaps between nanowires as small as 12 nm. This fabrication process combined high-resolution electron-beam lithography with photolithography. Although this work was motivated by the potential of increased detection efficiency with higher fill-factor devices, test results showed an unexpected systematic suppression in device critical currents with increasing fill-factor.

Index Terms—Critical current, detection efficiency, fabrication, single-photon detectors.

I. INTRODUCTION

SUPERCONDUCTING nanowire single-photon detectors (SNSPD) are extremely fast detectors with ~ 30 ps timing jitter [1], [2] and sub-5-ns reset times [3], [4]. SNSPDs also have low dark-count rates [5] and no after-pulsing effects. The combination of these properties makes the SNSPD a suitable detector in applications such as quantum key distribution [6], free-space optical communication [7] and VLSI testing [8].

The best detection efficiency (DE) of SNSPDs for 1.55 μm wavelength photons was reported as 57% [9]. While this performance is sufficient for most applications, further improvement of the device DE would be beneficial to current applications and could also enable new applications such as linear-optics quantum computing which require detectors with close to 100% DE [10]. As the detector DE is a product of (1) A , the absorptance of light in the device active area, and (2) P_r , the probability of resistive state formation given an absorption event, maximizing the device absorptance would provide further increase in DE.

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We previously demonstrated an increase in DE to 57% that was achieved by adding an integrated optical cavity on the detector and an anti-reflection coating on the back of the substrate [9]. The effect of these modifications was to increase the absorptance by a factor of ~ 2.5 relative to the original device. The fill-factor of the devices used in that experiment was $\sim 45\%$.

Currently there has been no systematic investigation on the effect of increasing the device fill-factor beyond 50% for SNSPDs sensitive to 1.55- μm -wavelength photons. Previous devices made using electron-beam lithography EBL and plasma etching were typically ~ 100 -nm-wide with $\sim 50\%$ fill-factor [11]–[15]. Recently, Delacour *et al.* [16] demonstrated a novel fabrication process using local oxidation with an atomic-force microscope to achieve 80% fill-factor SNSPDs with 270-nm-wide nanowires. However, the authors did not compare the performance of devices with different fill-factors.

In this paper, we report on a different fabrication approach to increasing the absorptance by increasing the device fill-factor. As shown in the calculations in Fig. 1, an absorptance $> 90\%$ can be achieved with a 90% fill-factor device, for the case back illumination of devices and in the presence of an optical cavity. This high absorptance will be crucial to achieving higher DEs in future devices.

Motivated by this extra absorptance afforded by higher fill-factor devices, we performed an experiment to observe this effect. We fabricated 100 devices on a single chip with fill factors ranging from 40% to 88%. The nanowire widths were kept constant at 90 nm in all devices, to maintain a constant P_r as the fill-factor was varied. Our fabricated devices had gaps in NbN as small as 12 nm, corresponding to fill-factors of 88%. To achieve this patterning resolution, we developed a process using high-resolution EBL with high-contrast cold development of poly-methyl metacrylate PMMA resist [17], followed by pattern transfer into 5-nm-thick NbN by reactive-ion etching.

We observed that the critical currents of the devices were systematically decreasing with increasing fill-factor. The cause of this suppression is currently not well understood but will be further investigated. As we could not bias the high fill-factor devices beyond their suppressed critical currents, their DE values were not as high as we had expected. Nonetheless, as expected, at bias currents just below the suppressed critical currents, the high fill-factor devices had higher DEs than the low fill-factor devices.

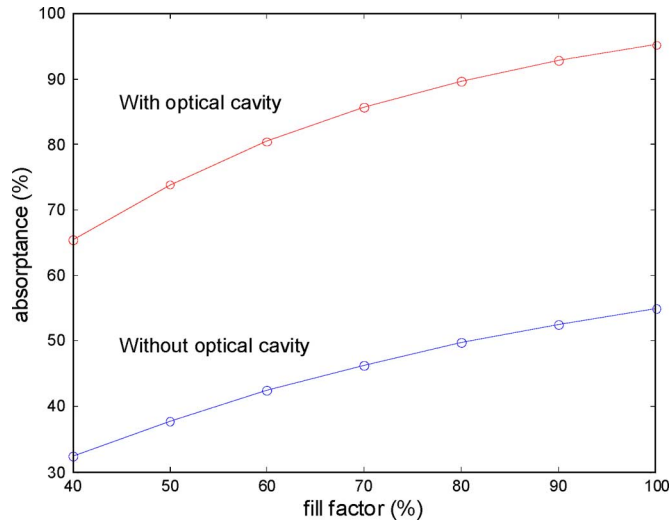


Fig. 1. Calculated absorbance vs. fill factor for the cases with and without an optical cavity for a 5-nm-thick NbN film on sapphire. An increase in absorbance by a factor of ~ 2 could be obtained by the addition of an optical cavity. An extra increase in absorbance of 30% could be obtained, going from 45% to 90% fill factor devices.

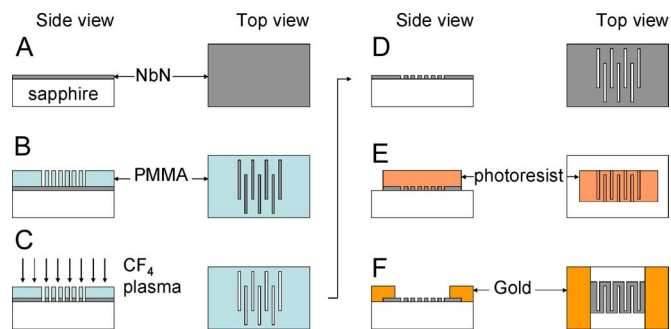


Fig. 2. Process flow for fabricating SNSPDs with fill factors ranging from 40% to 88%. The processes are as follows: (a) Starting material was 5 nm NbN on R-plane sapphire. (b) EBL of PMMA followed by resist development. (c) Reactive-ion etching. (d) Removal of PMMA, (e) Aligned photolithography and (f) Metal deposition for defining contact pads using a liftoff process.

II. EXPERIMENT

The devices were fabricated in the NanoStructures Laboratory at MIT using the process flow shown in Fig. 2. The starting material was a 5-nm-thick NbN on R-plane sapphire, grown at Lincoln Laboratory, cleaved to 1-cm-square chips and rinsed in acetone. We spin-coated 2200 k molecular weight poly-methyl methacrylate (PMMA) and baked the chip at 160°C on a hot plate for 8 mins. The thickness of PMMA after the bake was measured to be ~ 80 nm.

We used a Raith 150 EBL tool at 30 kV acceleration voltage to pattern interdigitated lines as shown schematically in Fig. 2(b). The pattern layout was designed to achieve gap widths ranging from 135 nm to 10 nm while maintaining a constant nanowire width of 90 nm, and detector active area of $3 \times 3 \mu\text{m}^2$, which resulted in devices with fill-factors ranging from 40% to 90%. We then developed PMMA using a high-contrast cold develop technique described in [17]. Using this process, the chips were developed in a 3:1 ratio of isopropyl alcohol (IPA): methyl isobutyl ketone (MIBK) at -15°C for 25 s and blown dry with a nitrogen gun.

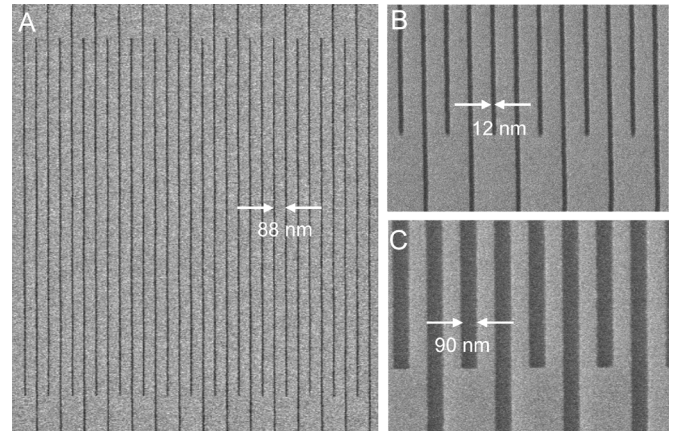


Fig. 3. Plan-view scanning electron micrographs (SEMs) of lines etched into NbN forming a meander structure. (a) SEM showing a $3 \mu\text{m}$ square meander with $\sim 90\%$ filling factor consisting of nanowires of 90-nm width and 12-nm wide gaps (dark lines). (b) SEM image of an enlarged view of a portion of the meander in (a) showing uniform linewidths and low line edge roughness. (c) SEM image showing a portion of a meander with 50% fill factor.

As shown in Fig. 2(c), the pattern was transferred into the underlying NbN using CF_4 plasma reactive-ion etching RIE at 100 W power and 10 mT pressure for 1 min. The PMMA thickness after etching was measured to be ~ 40 nm.

PMMA was stripped off the chip as shown in Fig. 2(d) by immersing the sample in 1-methyl-2-pyrrolidone (NMP) solvent in an ultrasonic agitator at room temperature for 5 mins. At this point in the process, the successful pattern transfer into NbN could be inspected by directly imaging the NbN in a scanning electron micrograph SEM as shown in Fig. 3.

We performed an aligned photolithography exposure of Shipley S1813 photoresist to mask only the central portion of the interdigitated lines as shown in Fig. 2(e). The unmasked regions were etched using CF_4 plasma RIE, thus creating a meander structure in the NbN film. The photoresist was then stripped using the same process for stripping PMMA as described above.

After a second aligned photolithography step, gold metal pads were deposited on the sample by electron-beam evaporation followed by a liftoff process as described in [14].

The devices were tested at MIT Lincoln Laboratory, using the procedures and apparatus discussed in detail in [9]. Briefly, the devices were cooled to as low as 1.8 K inside a cryogenic probing station. Electrical contact was established using a cooled $50\text{-}\Omega$ microwave probe attached to a micromanipulator, and connected via coaxial cable to the room-temperature electronics. We counted electrical pulses from the detectors using low-noise amplifiers and a gated pulse counter. To optically probe the devices, we used a 1550-nm mode-locked fiber laser (with a 10-MHz pulse repetition rate and ≤ 1 -ps pulse duration) that was attenuated and sent into the probing station via an optical fiber. The devices were illuminated from the back (through the sapphire substrate) using a lens attached to the end of the fiber which was mounted to an automated micromanipulator. The focal spot had a measured e^{-2} radius of $\sim 25 \mu\text{m}$. The detection efficiency of devices were calculated by taking the ratio of measured photon counts (after subtracting background

counts) to the number of photons incident from the laser on the $3 \times 3 \mu\text{m}^2$ active-area of the devices in a given time window.

III. RESULTS

A. Fabrication Results

The detector structures were imaged in a scanning-electron microscope after pattern transfer and PMMA removal. Fig. 3 shows some of the images from the detectors. Meanders with constant wire widths of 90 nm were fabricated with fill-factors ranging from 40% to 90% in steps of 10%.

B. Test Results

The data presented here were obtained from devices on a single chip. However, measurements done on two other chips, fabricated on separate runs, also show similar suppressions in critical currents with increasing fill factor.

Device resistances at room temperature and inductances at 1.8-K were measured. The device resistance and inductance, which was dominated by the kinetic inductance of the nanowire, both scaled with wire length. For a constant active area, increasing the device fill-factor resulted in a longer total nanowire length, hence higher device resistance and inductance. The tight clustering of data points in the plot of resistance vs. inductance shown in Fig. 4(a) is evidence for the device uniformity within a group of devices with the same nominal fill-factor. Furthermore, with the exception of the data for the 88% fill-factors, the linear fit to the data passing through the origin (similar plot in [4]) shows the expected constant resistance-to-inductance ratio. The data also agrees well with calculated values of resistances and inductances based on the total length of the nanowires. Note that although the data points for the 88% fill-factors were poorly fitted here, corresponding measurements on another chip showed good agreement.

As the width of the nanowires was kept constant, we expected their critical currents to also be constant across different fill-factors. However, the data presented in Fig. 4(b) show that the measured critical currents had an unexpected, systematically decreasing trend with increasing fill-factors. We see that the 88%-fill-factor devices had critical currents that were suppressed by $\sim 35\%$ relative to the 40%-fill-factor devices.

This large suppression in critical currents was *not* due to patterning errors, which would cause an undesirable reduction in wire width. Scanning electron microscopy SEM inspections of the wires verified that wire widths were uniform at 90 ± 5 nm across all fill-factors. However, the drastic critical-current reduction required a discrepancy in wire width of 32 nm which clearly was not observed in the SEM inspections. Furthermore, such patterning errors, if they occurred, would also cause observable discrepancies between the measured vs. calculated inductances and resistances, which was not present, as shown in Fig. 4(a).

The systematic critical current suppression was unlikely to be the cause of random constrictions in the nanowires [18], which would exhibit a larger scatter in the data points than is shown in Fig. 4(b). Furthermore, random constrictions should affect all fill-factors equally, unlike the systematically larger suppression of critical current with increasing fill-factor observed.

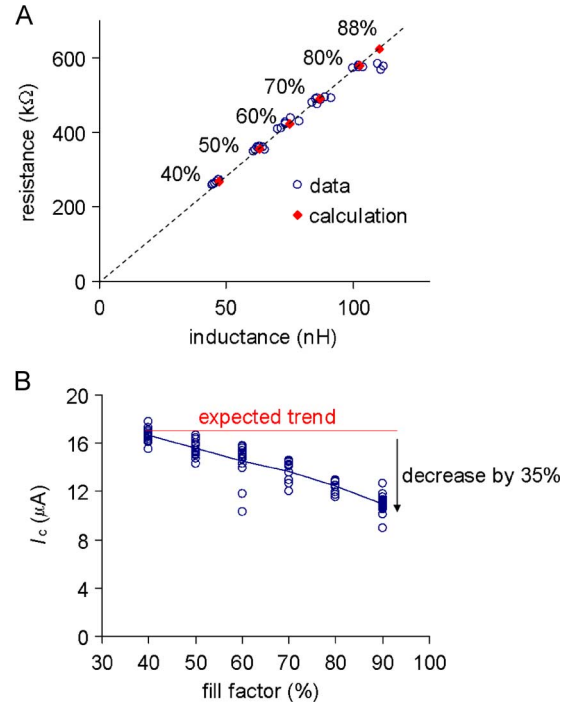


Fig. 4. Electrical characterization of devices with different fill factors. Open circles are data points for different devices on the same chip. (a) Resistance vs. vs. inductance plot showing good device uniformity for each fill factor type. Calculated values based on nanowire length agree well with measured data. (b) Critical currents for devices with different fill factors showing an unexpected decrease in critical currents with increasing fill factor.

Instead, some new effect is suggested by this systematic suppression in critical currents. It is possible that these devices, in the new regime of sub-100-nm gaps between the nanowires, were exhibiting an effect that has not been previously investigated. Some hypotheses that could explain this effect are discussed in the next section.

The curves of DE vs. bias current were measured for each fill-factor across multiple devices on a single chip. The data from these measurements are shown in Fig. 5 after scaling the horizontal axis of each curve by a factor C , such that the low-current portions of the curves lined up. Scaling the curves enabled clear comparison across fill-factors and removed random variations (due to critical current density variation and/or linewidth variations) across devices. The value of C ranged from 0.8 to 1.

Although the low-current portions of the curves looked identical, the curves diverged beyond $\sim 12 \mu\text{A}$. The DE curves of higher fill-factor devices were higher than those for lower fill-factor devices. As a result, for a given bias current, the DE values increased with increasing fill factor. However, due to the suppression in critical currents, the high bias-current portions of the DE curves were measurable only for the low fill-factor devices. Hence, the high fill-factor devices could not exhibit as high a DE as they should if their critical currents were not suppressed. The DE curves of the higher fill-factor devices ended at lower current values, as indicated by the arrows in Fig. 5(a).

The highest device DE obtained was for a 60%-fill-factor device having a DE value of $\sim 20\%$, which is comparable to the DE achieved with the previously established HSQ process [9], [14], with back illumination, and without an optical cavity or an

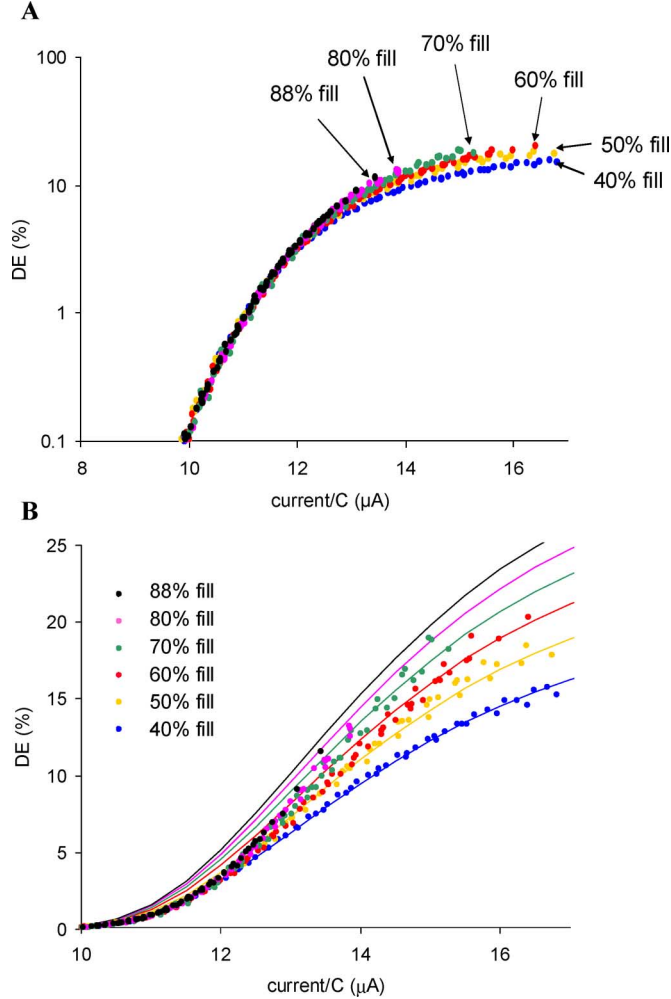


Fig. 5. *DE* measurements for different bias currents that were scaled to line up the data points at the low current values. Increasing fill factor was accompanied with higher trend in the *DE* curves. (a) Arrows indicate the points on each curve where the *DE* was highest for each fill factor group. (b) Linear scale plot of *DE* vs. current. The blue solid line was a fit to the lowest fill-factor data points. The other solid lines were obtained from scaling this of this fit by scale-factors calculated from the expected increase in absorptance.

anti-reflection coating. This suggests that the new process was compatible with NbN.

The amount of increase in *DE* with fill-factor was in close agreement with the expected increase due to the resulting increase in absorptance. For clarity, we show in Fig. 5(b) the same data as in Fig. 5(a) but on a linear scale for the *DE* axis. We first obtained a fit to the data for the 40% fill-factor devices, as shown in the solid blue line, using the phenomenological equation $DE = M \exp^{-NI^P}$ where *M*, *N* and *P* were fitting parameters and *I* was the bias current of the device. The fit to the 40% fill-factor devices was obtained using values of $M = 21.5$, $N = 1.644 \times 10^6$, $P = -5.5$ and *I* in units of μA . This phenomenological equation was also found to fit data well across a broad variety of devices from other measurements. If the detection efficiency of devices with different fill factors was only affected by the absorption, the detection efficiency vs. bias current curves should be identical except for different scale factors, *M*, which correspond to the expected

differences in absorptance. Consequently, we scaled the fit obtained from the 40% fill-factor devices along the *DE* axis by scaling-factors that were calculated from the fractional increase in absorptance due to increasing fill-factor. The calculations, as presented in Fig. 1, were done by solving plane-wave propagation of 1.55- μm -wavelength light through layered media consisting of sapphire, NbN and vacuum. We approximated the nanowire plane as a continuous layer having an effective relative permittivity ϵ'_{NbN} that was the average of that of an unpatterned NbN film ϵ_{NbN} and vacuum $\epsilon_{\text{vac}} = 1$, i.e. $\epsilon'_{\text{NbN}} = (\text{fill} - \text{factor})\epsilon_{\text{NbN}} + (1 - \text{fill} - \text{factor})\epsilon_{\text{vac}}$. For the case of parallel polarization, where the electric field was parallel to the length of the nanowires, this calculation exactly matched the results of the finite-element analysis reported in [19]. The following were the scaling factors obtained for the corresponding fill-factors in parentheses: 1 (40%), 1.16 (50%), 1.3 (60%), 1.42 (70%), 1.53 (80%) and 1.61 (88%).

IV. DISCUSSION

The *DE* of 60%-fill-factor devices fabricated using this new process was comparable to the best *DE*s of devices made using a previous process which utilized HSQ as the EBL resist [14]. This similarity in device performance is an indication that the new fabrication process did not cause material degradation or device damage.

The systematic suppression in critical currents with increasing fill-factor was an unexpected result. SEM inspections of the nanowire widths from different fill-factor meanders showed that they were uniform to within 10% of each other. While the *DE* measurements seem to suggest that the high fill-factor meanders were constricted, the critical current measurements show a small scatter in the data which is not characteristic of constricted devices.

We hypothesize that the systematic suppression in critical currents could be due to one of several possibilities: (1) increase in local current densities at the bends of the meander, (2) stronger electromagnetic coupling between nanowires that are closely spaced, (3) constrictions along the nanowire, or (4) noise in the fabrication process.

Local increase in current density as the current makes a 180° turn at the bends of the meander is one plausible explanation. We would expect the supercurrent to follow the path of least inductance, which might result in a non-uniform current density at the bends. Such an effect might cause an apparent constriction that systematically becomes more severe for tighter bends.

One would also expect the electromagnetic fields of a nanowire to affect the current distribution in neighboring nanowires more strongly when the gaps between them are reduced. The magnetic fields are highest at the edges of the wires and decreases as a function of approximately 1/distance away from the edges. However, our calculations show that the magnitude of the magnetic fields generated by a nanowire is several orders of magnitude smaller than the critical magnetic field of NbN.

As explained above, the small scatter in the critical-current measurements was uncharacteristic of constrictions. Although unlikely, constrictions along the nanowire might also explain

the critical-current suppression. Since the higher fill-factor devices had longer nanowires, the probability of defects along the nanowire length might also increase with fill-factor. We have seen that devices with larger active areas ($10 \times 10 \mu\text{m}^2$) had a higher probability of large constrictions [18]. If we consider a fixed density of defects in the NbN film, a larger device, which also samples a larger film area, will have a higher probability of defects. However, as the active area was kept constant, the distribution of defects should be the same for all fill-factors, which suggests a similar distribution of critical currents. Hence, constrictions could explain our observations only if they arose not from the film, but from the lithography.

Finally, there may be effects in the fabrication process that, although not apparent at this point, may result in more variation in nanowire cross-sectional areas for the higher fill-factor devices. Although SEM images did not show any visible non-uniformity in the width of the wires, there may be random process variations, e.g. in the etching, that caused variations in the thickness of the wires.

V. CONCLUSION

We have developed a fabrication process using high resolution EBL of PMMA to make detectors with fill-factors as high as 88% while maintaining the nanowire width of ~ 90 nm.

We observed a decrease in critical currents with increasing fill-factor which was not caused by a decrease in the nanowire widths or by random constrictions along the nanowire. Future experiments will investigate the cause(s) of this systematic suppression in critical currents.

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