Superconducting nanowire electronics in Magnesium Diboride

Implementation of a Python-based library for nanoscale fabrication of superconducting devices and circuits. Definition of a process fabrication flow for patterning Magnesium Diboride at the nanoscale. Characterization of nanowire switching events over a large temperature range.

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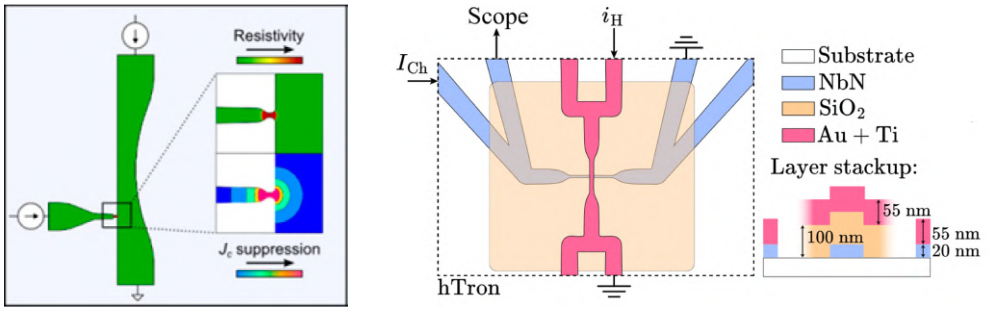
1 Introduction

In this thesis report, we will present the work we achieved over the past six months in the Quantum Nanostructure and Nanofabrication (QNN) group at MIT, under the supervision of Prof. Karl K. Berggren. The original idea behind this visit was initially quite vague, but we had one certainty: working on a process for fabricating nanowire-based devices in Magnesium Diboride.

Superconductivity is a quantum mechanical phenomenon in which a material can conduct electricity with zero resistance and expel magnetic fields, known as the Meissner effect. This state occurs below a critical temperature, where electrons form Cooper pairs. The superconducting order parameter is a complex quantity that describes the density and coherence of these Cooper pairs, which are essential for maintaining the superconducting state. [2]

The behavior and properties of superconductors are defined by two primary characteristic length scales that are the coherence length ξ and the London penetration depth Λ. ξ represents the length scale over which the superconducting order parameter is affected by external influences. Λ represents the distance over which an external magnetic field is exponentially damped inside the superconductor. When fabricating superconducting devices with feature sizes smaller than these characteristic lengths, nanoscale phenomena become significant. Such small dimensions allow the devices to exploit unique superconducting effects like kinetic inductance (the inertia of Cooper pairs), electrothermal suppression (control of superconductivity via heating effects), and current crowding (localized increases in current density). These effects can be harnessed to create high-performance superconducting devices for various applications.

Nanowire electronics is a rapidly growing field that leverages the properties of superconducting nanowires for a variety of applications, including quantum computing [11], sensing [22], and advanced communication systems [10]. In the QNN group, commonly studied superconducting devices are the nTron [15] (fig.1(a)), the hTron [1] (fig.1(b)), the Superconducting Nanowire Single Photon Detector (SNSPD) [3] (fig.2) or even simple nanowire constrictions. Their operating principle are all based on the switching event of a nanowire.



(a) (b)

Figure 1: Schematics of (a) a nTron (McCaughan and Berggren 2014)[15] and (b) a hTron (Karam et al. 2024)[12], taken from the group publications.

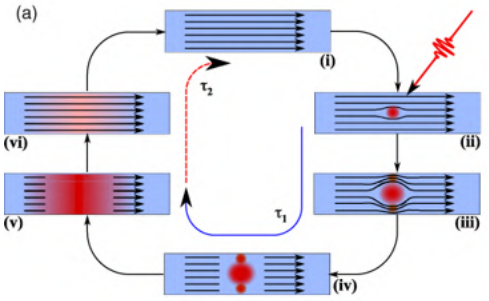


Figure 2: Conceptual representation of the operating principle of a SNSPD.[19]

Most commonly used superconductors for such applications are Niobium Nitride (NbN) or Niobium Titanium Nitride (NbTiN). These materials have been widely studied over time and many detectors and devices have been developed using them. However, the quest for materials that offer superior performance characteristics, notably in terms of the superconducting critical temperature, is always ongoing. Magnesium Diboride (MgB_2), discovered in 2001, represents an interesting alternative candidate. Its high critical temperature of 39 K [18], low normal state resistivity, and the facts that it is lightweight and made from elements that are abundant in nature make it a promising material[4]. Despite the great enthusiasm after its discovery, the difficulty of depositing thin films with high uniformity and low roughness slowed down the studies.

Recent progress have been demonstrated by (Kim et al., 2023) that achieve good uniformity (< 100 nm) and low roughness (< 0.5 nm rms) by co-sputtering Mg-B compound, capping it in a Boron layer and post-annealing to form MgB_2.[13] A collaboration established between QNN group and the JPL group allowed us to be provided with one full Si wafer with a 30nm thick layer of MgB_2 capped by 40nm of Boron.

Alternatively, (Charaev et al. 2024), as well in collaboration with the QNN, demonstrated single-photon detection using large-scale sensors in MgB_2 deposited with Hybrid Physical-Chemical Vapor Deposition (HPCVD) technique, and used helium ions to irradiate the devices.[5]

With this context in mind, we could see emerging necessary milestones to achieve in order to reach our goal: the fabrication of nanowire-based superconducting devices in Magnesium Diboride. First, define potential process flows of fabrication, taken in consideration the constrains relative to MgB2. Second, design a layout as useful and complete as possible to showcase and monitor the properties of the patterned MgB2 layer. Last, characterize the fabricated devices at cryogenic temperatures.

The report is organized in three sections following a logical order of presentation. We begin by presenting our work on building a Python library, called qnngds, that defines a common structure and experiments for generating nanowire electronics fabrication layouts. In a second time, we present and discuss the fabrication flow followed for patterning the designed layout onto our Magnesium Diboride sample, provided by JPL. Finally, we present the measurements performed on some superconducting nanowires that survived the fabrication.

2 Designing nanowire electronics

2.1 Introduction

Nanofabrication represents a pivotal area in modern technology, focusing on the creation of structures and devices on the nanometer scale. Remarkable advancements have been achieved in reducing feature sizes to just a few nanometers, driven by the escalating demand for miniaturized, high-performance devices across various sectors including electronics, photonics, and biotechnology. This relentless pursuit of smaller dimensions necessitates precise and sophisticated layout design to address the unique challenges posed by nanoscale fabrication. Designers must navigate issues such as quantum effects, material property variability, and fabrication limitations, all of which demand innovative strategies and meticulous planning to ensure the functionality and reliability of nanoscale devices.

To address the complexities inherent in nanoscale fabrication, layout geometry tools have become indispensable in the design process. These tools enable precise coding of the design, allowing for fine-tuned adjustability and stringent control over critical parameters. Layout geometry tools facilitate iterative design refinement, enabling rapid adjustments and real-time feedback, which are crucial for achieving the high precision required at the nanoscale. These tools not only enhance design accuracy but also streamline the development cycle, making it possible to achieve more reliable and high-performance nanoscale devices.

To facilitate the intricate process of nanoscale layout design, PHIDL (Python-based layout and geometry creation for nanolithography) has emerged as a highly effective tool. Introduced by McCaughan et al. in their 2021 publication [16], PHIDL offers a robust platform specifically tailored for creating precise and complex nanoscale geometries. This tool has become a cornerstone in our group's design efforts, providing a versatile and powerful means to code and adjust our layouts with proper control over critical parameters, taking into account current crowding principles outlined by John R. Clem and Karl K. Berggren in their work on geometry-dependent critical currents in superconducting nanocircuits [7].

Despite the advantages offered by PHIDL, our group still faces a significant challenge: the absence of a comprehensive library to standardize our layouts. Such a library would include organized layers, test structures, and a repository of devices and circuits, ensuring consistency and efficiency across our design processes. Establishing this library is the focus of this section, aiming to streamline our design workflow, promote best practices, and enhance the reproducibility and reliability of our nanoscale fabrication projects.

2.2 Presentation of qnngds

QNNGDS is an open-source CAD tool in Python for creating GDS layouts destined for the fabrication of nanowire electronics. It regroups devices and test structures to be directly added to a layout, as well as useful functions for building new circuits. It was thought to be a package for the QNN group, in which students can share the designs they have already made. Therefore, the package is organised so that the shared designs can easily be reused and adapted by others.

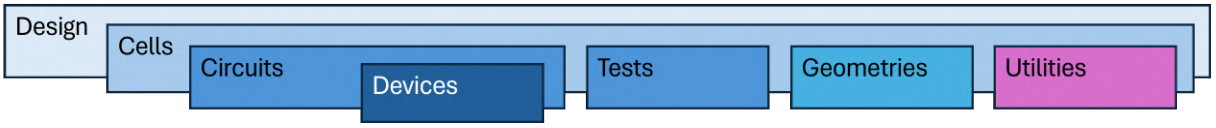


Figure 3: Hierarchy of the modules in QNNGDS

- Design: contains classes from which a complete design can be built. The class inputs are the basic parameters of the chip. Its methods are pre-built cells and tools for distributing and managing the cells over the chip.
- Cells: is a library of cells pre-built, that are called by the Design's classes. Each cell contains a text, border marks and an experiment (circuits, devices, or tests) connected to pads for external connection.
- Circuits: is a library of circuits made of devices.
- Devices: is a library of basic devices like nTron, hTron, nanowires, resistors etc...
- Tests: is a library of test structures that help through the fabrication process and characterization.
- Geometries: contains useful shapes/geometries that are not available in Phidl or has been adapted from it for special use case.
- Utilities: contains useful tools for building cells and circuits.

Figure 4 displays an example of the modules used to build a design. This example particularly enlighten the fact that devices, circuit, test etc exist by themselves. The package is made as modular as possible so that elements can be shared and reused as easily as possible. This is very different than getting some other student's final layout and extracting from it some experiments. The package is made as a library, but is not an archive.

The complete API can be found on qnngds documentation directly. It describes each element available in the package, its input arguments and output.

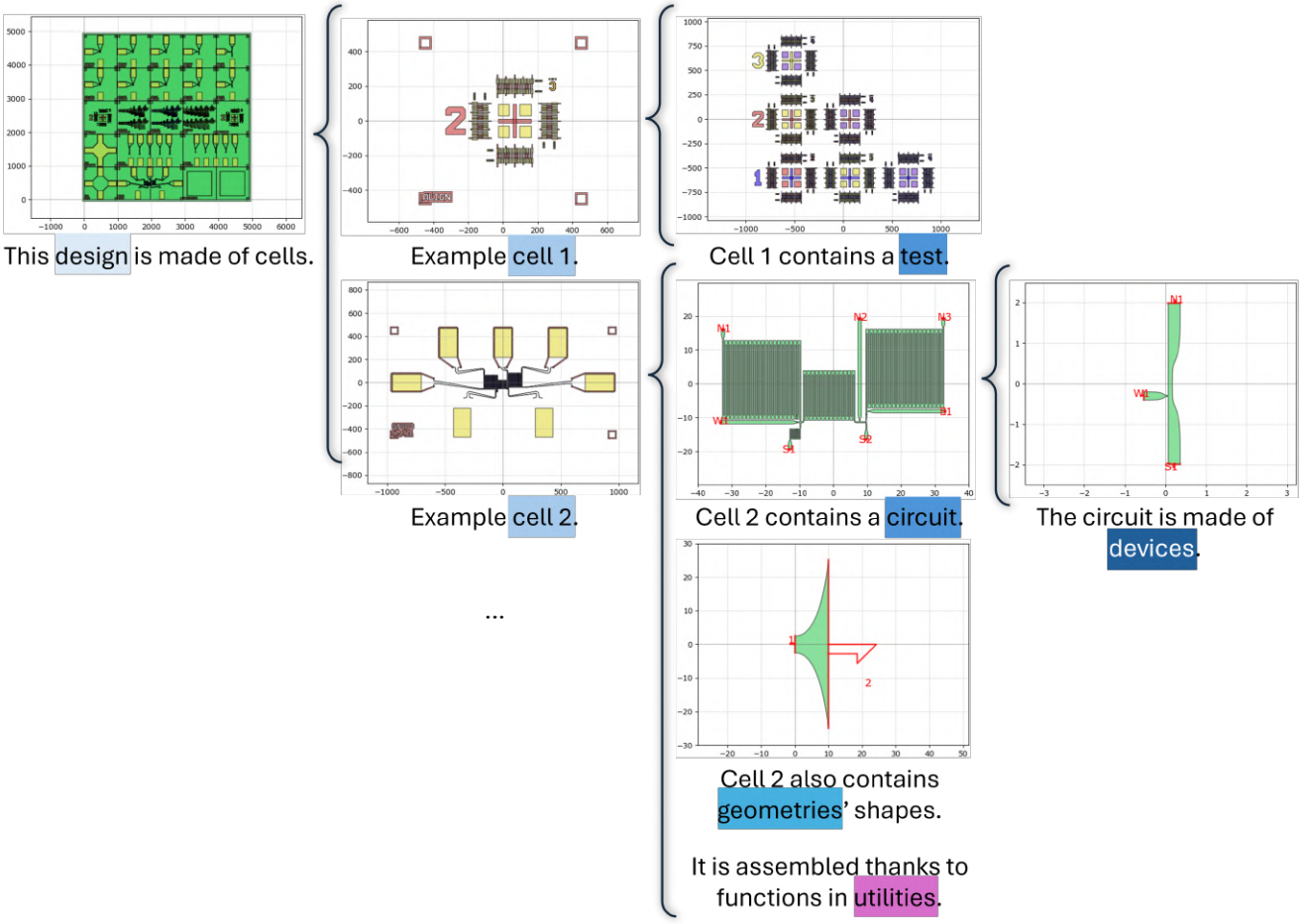


Figure 4: Example of the modules entanglement.

2.3 How to use the package

In this section, we will briefly describe how to use the package. Again, we invite the reader to refer to the documentation for a more complete support, in particular we invite them to check the tutorial getting started for first time users and the developers' documentation for first time contributors or maintainers of the package.

As mentioned previously, the package was built in order to ease sharing designs and hence make the group knowledge profitable and accessible to all. The current existing version of the package should be considered a structure for a future robust tool for designing nanowire electronics. It is expected that others will use qnngds to create and structure their designs and then hopefully contribute with their new inputs.

Below, we go through the steps someone would follow when willing to create a new layout with qnngds.

1. Setup and package installation
2. Define the layout's purpose and deduce what it should contain
3. Code the missing circuits/devices, not from scratch
4. Contribute

2.3.1 Setup and package installation

A good practice before coding a new GDS layout is to have a specific environment for this layout only. The virtual environment can be created in the folder created for the purpose of the project. This assures the code can always be compiled and adapted if needed as it stores the correct versions of the packages used at the time of the design creation.

```
python -m venv .venv/your-env-name
.\.venv\your-env-name\Scripts\Activate
```

In this environment, can be installed qnngds, preceded by gdspy (required to be installed first). For windows, what works best is to install a pre-built wheel of gdspy and run:

```
pip install path/to/gdspy-1.6.12-cp38-cp38-win_amd64.whl
```

On Linux, the installation is simpler:

```
pip install gdspy
```

Finally:

```
pip install qnngds
```

A new python file that will serve for the layout can now be created and qnngds imported.

2.3.2 Define the layout's purpose and deduce what it should contain

Before trying to make any layout, it is very useful to have a clear idea of the process flow that will be used to fabricate the chip. Indeed, knowing the challenges behind the process is knowing the critical parameters of the design as well as the type of test needed to monitor the fabrication.

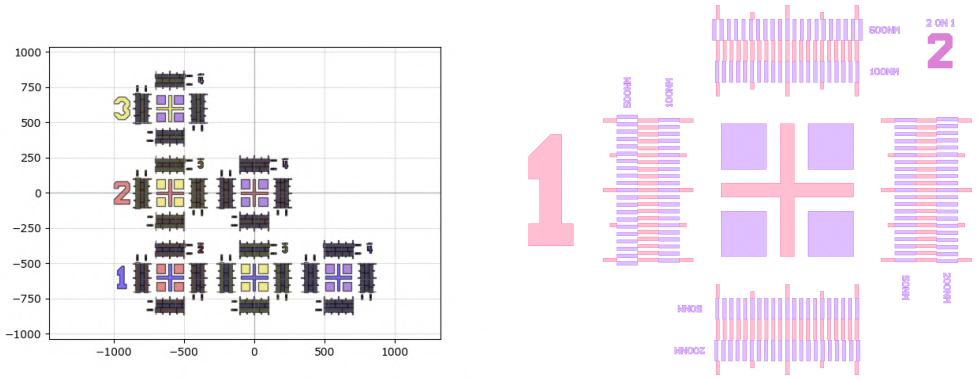
Unfortunately there is no simple and small cell that can be added to any chip to monitor its fabrication. However, below we will discuss some test structures and the cases where they might be useful to integrate in a design.

Alignment marks: The alignment marks displayed in figure 6 are made for both manually aligning layers together (using the center cross) and to monitor the error in the alignment after the exposure (combs on the outsides). Those combs are Vernier caliper of 50, 100, 200 and 500nm oriented vertically and horizontally. Figure 5 is an example of what can be seen on one caliper after the alignment of two layers (in pink and purple). The procedure to properly read such a caliper is as follow:

1. Start by locating the caliper that spreads over the first layer. In this case, it is the 500nm caliper (on the left).
2. Find the two lines from layer one and two that are aligned. In the figure, they are marked by the black rectangle.
3. Count the number of marks it makes from the center (black line). Here we count +7.
4. The vertical error of alignment here is $\Delta = +7 \times 500\,\text{nm} = +3.5\,\mu\text{m}$.

Figure 5: Example of a Vernier caliper

Both the vertical and horizontal measures, on two different alignment marks situated as far as possible on the sample, have to be taken for a complete reading of the alignment of two layers.



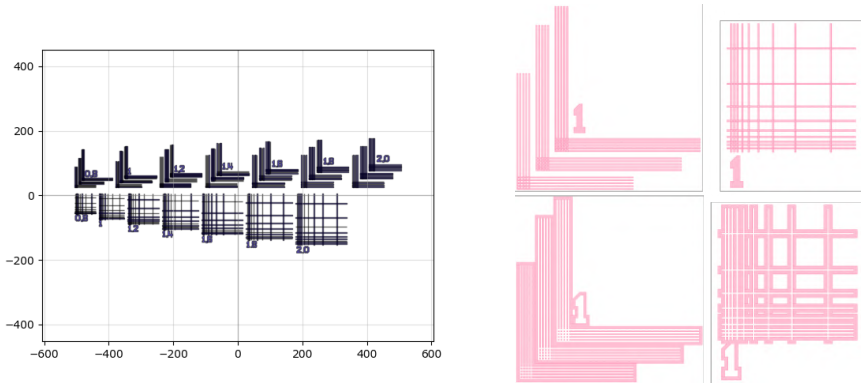
(a) (b)

Figure 6: Alignment marks. (The scale in (a) is in µm.)

Points to be considered before adding alignment structures:

- What is the most appropriate resolution of the vernier calipers? Note that they do not depend on the resolution of the exposure tool but only on the achievable precision of the alignment.
- Alignment marks can quickly take a large place on a sample (above all if it is a piece). Its main advantage is that it optically gives the misalignment even if this value is not optically resolvable (sub-microns). If the tolerance of alignment between two layers is larger than what can be optically resolvable, the need to precisely know the alignment error may not win over the space it can make available. However, if the tolerance is smaller, having calipers represent a simple pass/fail test without having to take the sample with its resist to a SEM.
- (These marks are particularly adapted for photolithography. However, they would work as well to evaluate the misalignment between a high and a low current e-beam exposure for example; as long as the structures are outlined/inverted to limit the writing time.)

Resolution test: Resolution structures, as shown in figure 7, can help determining the resolution of an exposure, but also compare how it evolves through the process: transfer to a hard mask, or transfer to a film etc. The shapes of the structures are made to evaluate as widely as possible what the process impact is on the resolution. Some differences might be observed in denser or lighter regions. Drawing a single isolated line is often not enough to determine if the process successfully reaches this resolution. Similar considerations apply to positive and negative exposures, those structures inverted or not do not carry the same information.



(a) (b)

Figure 7: Resolution test. (The scale in (a) is in µm.)

Points to be considered before adding resolution tests:

- To choose an informative range of resolutions to test, it is worth asking ourselves two questions. What is the lowest resolution expected from the exposure? What is the lowest resolution required for the circuit/devices to work?
- Consider the fact that those structures, unlike the alignment calipers, have to be imaged at the scale they are testing, i.e. under SEM for sub-micron resolution. If the sample cannot be imaged for some reasons (an isolation layer for example), the structures won't be useful either.

Van der Pauw test: Figure 8 gives the simplest geometry that can be used as a Van Der Pauw (VDP) structure for determining parameters like the sheet resistance or the Hall coefficient of a sample. The conditions required for a structure to be used as a VDP are: a 2D sample, a solid shape (i.e. no holes) and that the 4 electrodes/contact points are placed on its parameter and are at least an order of magnitude smaller than the area to probe. It differs from a standard 4-points measurement by the fact that the measure results of an average of the material, making a difference for anisotropic materials.

Theoretically, measuring the resistances $R_{12,34} = \frac{V_{34}}{I_{12}}$ and $R_{23,41} = \frac{V_{41}}{I_{23}}$ is sufficient to determine the sheet resistance R_S after Van der Pauw formula, given in equation 1. [20]

$$e^{-\frac{\pi R_{12,34}}{R_s}} + e^{-\frac{\pi R_{23,41}}{R_s}} = 1 \tag{1}$$

However, performing additional resistances measurements (reciprocal and with reversed polarity) is a good practice and allows for more accurate value of the sheet resistance. Only when $R_{vertical} = R = R_{horizontal}$, i.e. in the case of an isotropic material, the sheet resistance is given by:

$$R_s = \frac{\pi R}{\ln 2} \tag{2}$$

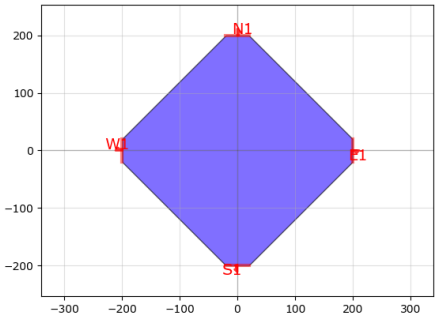


Figure 8: Van der Pauw structure. (The scale is in µm.)

Points to be considered before adding Van Der Pauw structures:

- Are they multiple conductive layers stacked? Does the process flow allow for the measurement of the specified layer?
- Is the area probed representative of the rest of the sample? Where and how many of those structures to place?

Testing devices: Apart from the test structures, individually testing the devices that will be integrated in a circuit is crucial. Again, the trade-off is between the available space and the understanding of the sample. Cells containing a single nTron, simple constrictions, SNSPD or any kind of existing device can be added to a layout in order to test them. Figure 9 shows single devices (in purple) and the place it represents when integrated in a cell with contact pads (in yellow). This is a great example of the challenges behind the integration of nanoscale devices.

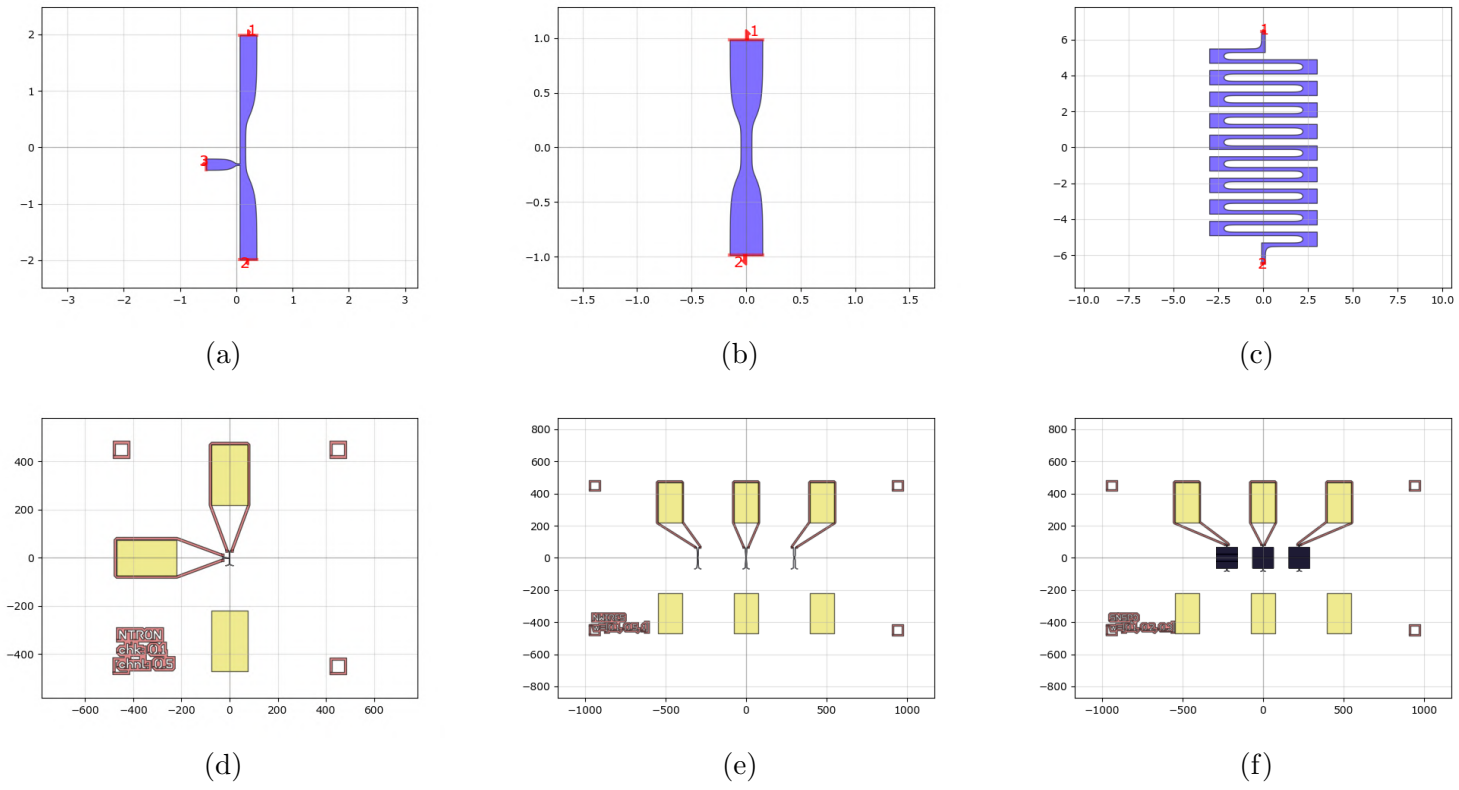


Figure 9: (a) A nTron, (b) a constriction, (c) a SNSPD and (d, e, f) their integration in a cell for individual testing. (The scales are in µm.)

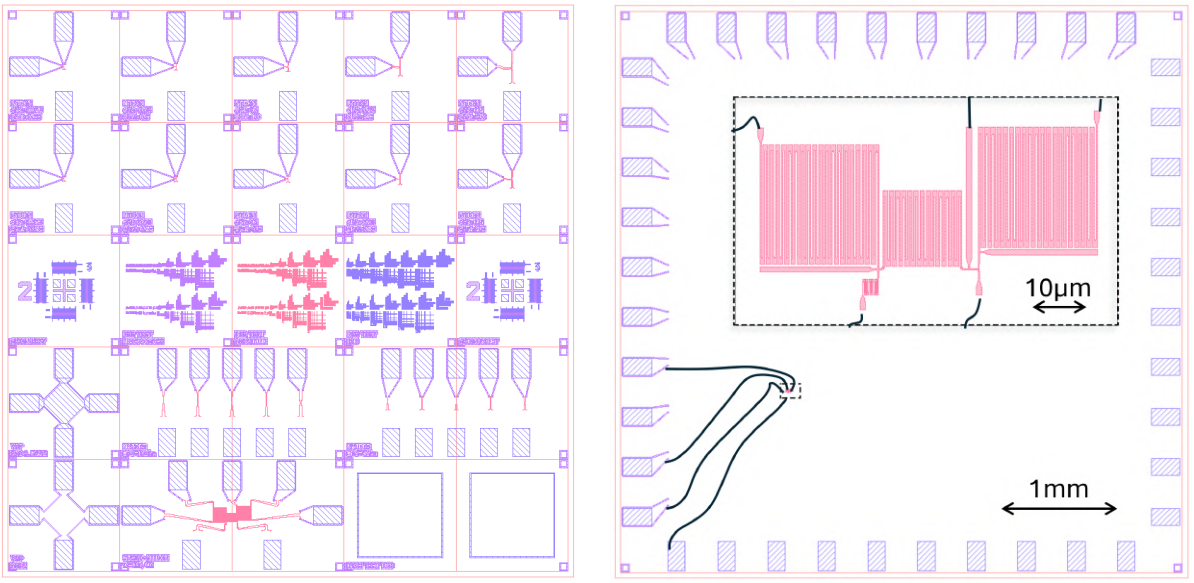
2.3.3 Code the missing cells, not from scratch

It is highly probable that any user of the current version of qnngds would find the package incomplete. As explained previously, this version represents a structure for a library to be completed. However, in addition to being a library, it also already offers tools for building layouts particularly targeting nanowire electronics designs. Below we give a list of functions useful to build a cell from a circuit and how they can be used.

die_cell(): Conventionally, samples that require to be wire-bonded almost always have their connection pads located on its perimeter for practical reasons. Currently, qnngds offers one function called `die_cell()`. It takes as inputs the number of pads on each edge (N, S, E, W) and the ones connected to ground. In most applications in the group, several small experiments need to be performed on a single chip (like testing a single nTron for example). Hence, the design class has been built so that 1 layout is made of several cells, 1 cell is made of 1 experiment (a single nTron, a resolution test, an entire circuit etc...) and its contact pads on the edges of the cell. This is the case described in figure 10(a).

However, the package is flexible and nothing prevents users to build a layout with pads

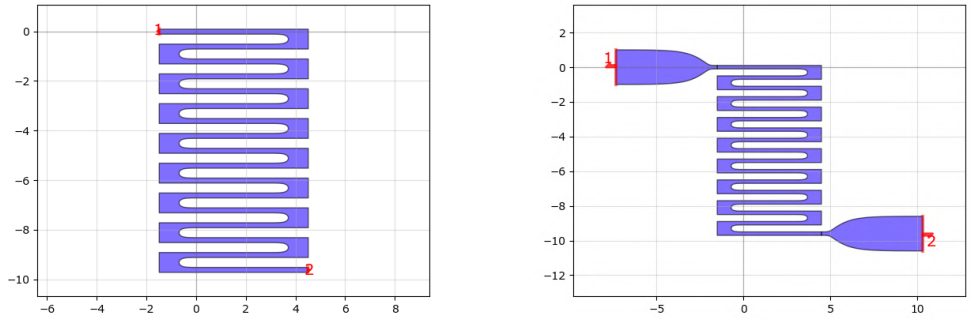
on the edges. What is needed: create a `die_cell()` with the size of the piece, add the circuits/devices/structures to test and route them to the pads. Figure 10(b) is a schematic of a single small circuit routed to the edges of a 0.5cm chip. It is quite straightforward from this schematic that for micrometer-scaled experiments, routing to the edges of a chip is very complex. Using such a configuration makes sense for full (i.e. bigger) circuits.



(a) (b)

Figure 10: (a) Typical layout containing several devices and tests on a 0.5cm x 0.5cm piece. The layout represents well how the package is built: a chip (pink frame) divided in multiple cells (all integers of unit cell size) containing the experiments and the contact pads. (b) An example of the complexity it would represent to place and route a single simple circuit (SNSPD coupled to a nTron, with 3 inductors) in such a chip if the contact pads were on the edges, although possible.

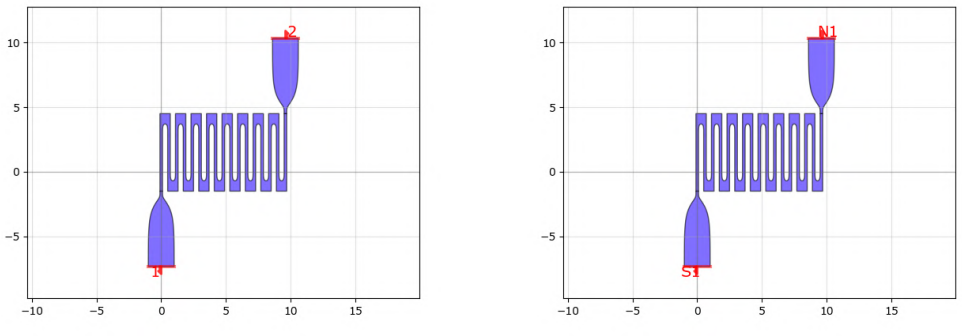
add_optimal_step_to_dev(): When willing to integrate any experiment to the layout, it is crucial in nanowire electronics to consider current crowding [7]. This function takes a device and adds to its ports the geometry `optimal_step()` provided in Phidl. Figure 11 gives an example of how to use this function on a SNSPD.



(a) (b)

Figure 11: A SNSPD device out of `qnngds.devices.snspd.basic()` library (a) before and (b) after passing applying `add_optimal_step_to_dev()` function. (The scales are in µm.)

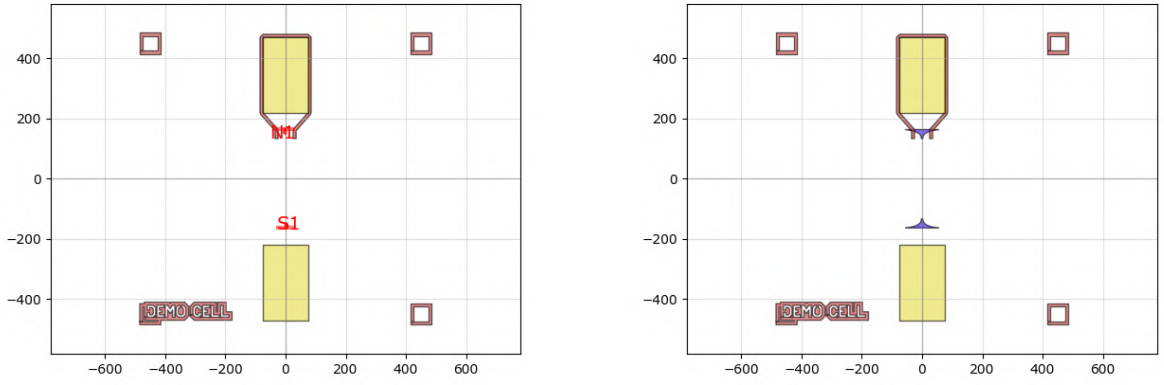
rename_ports_to_compass(): Once an experiment is ready to be integrated into a cell, its ports need to be connected to the contact pads. As shown in figure 12, this function takes the device in input and rename its ports with compass names based on its orientation (N, S, E, W followed by a number).



(a) (b)

Figure 12: A device (a) before and (b) after applying `rename_ports_to_compass()` function. (The scales are in µm.)

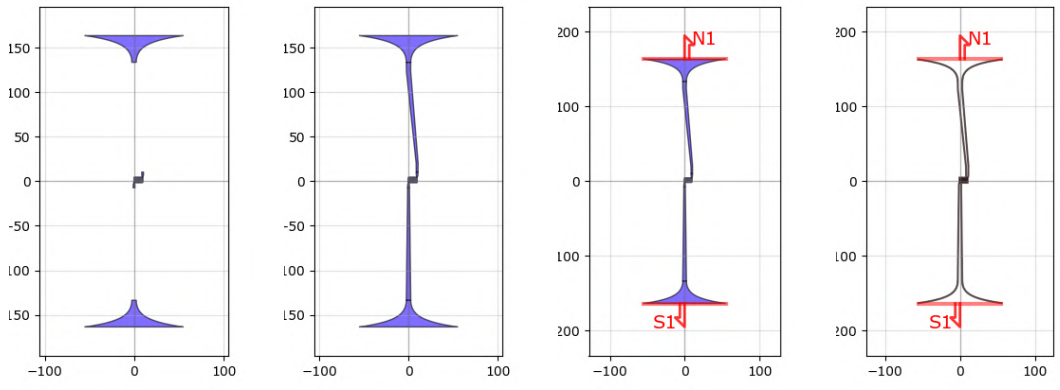
add_hyptap_to_cell(): E-beam lithography enables to go down to the nanoscale resolution making it the basis of nanowire electronics exposures. As a drawback, the exposure can easily take an important time even for small pieces and hence can be costly. For this reason, it is common to split the exposure of a single layer in two: one exposure for structures needing nanometers resolution and another one for bigger shapes like pads and text, done at higher e-beam current or using laser writing. Consequently, tapers shapes are added in the layout at regions where the lines is cut because of the switch in exposure. They account for the error in misalignment. This function takes a cell and creates at its ports the geometry `hyper_taper()` provided in Phidl. Figure 13(b) gives an example of the tapers (in purple) obtained when passing the `die_cell()` represented in (a).



(a) (b)

Figure 13: (a) A `die_cell()` and (b) the hyper tapers (in purple) created after running `add_hyptap_to_cell()` function. (The scales are in µm.)

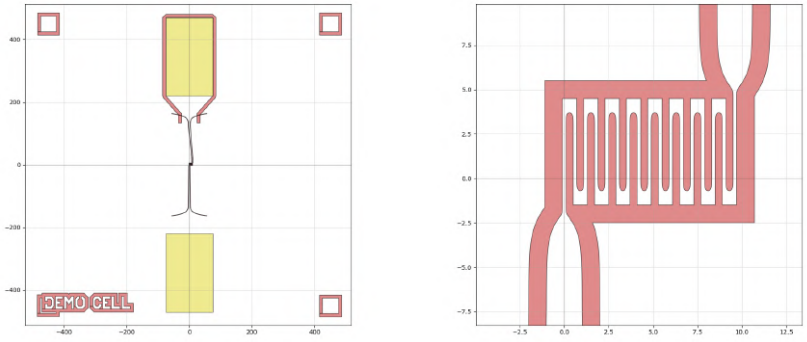
route_to_dev(): Finally, electrical connections need to be routed from the tapers to the device's ports. Phidl provides routing options wider than what `route_to_dev()` function currently allows; but it can be very useful when working properly, as shown in figure 14.



(a) (b) (c) (d)

Figure 14: An experiment in construction from (a) a SNSPD and hyper tapers to (b) the complete device routed with `route_to_dev()` function. In (c) and (d) is represented the process of outlining the experiment for e-beam positive exposure without outlining the device at its ports (in red). (The scales are in µm.)

Before the cell is fully ready, the device, routes and hyper-tapers often needs to be outlined for positive e-beam exposures. For this purpose, represented in figure 14(c and d), the function `outline()` from Phidl geometry can be used with the "`open_ports`" option. The ports of the final device composed of the experiment, the routes and the tapers (i.e. the ports to be ignored in the outline) are outputs of `add_hyptap_to_cell()`.



(a) (b)

Figure 15: The final result of the example followed in this section to underline the tools available in `qnngds.utility` module. (a) The complete cell and (b) a zoom on the device. (The scales are in µm.)

Note that the created cell is not necessarily optimized in terms of parameters and was only displayed to highlight the potential of the current tools offered. Also note that qnngds is not an equivalent of Phidl. The circuits and devices are still mainly assembled through Phidl's geometry toolkit and it is only after (at a higher level) that qnngds takes its part in the layout's design.

2.3.4 Finalize the layout

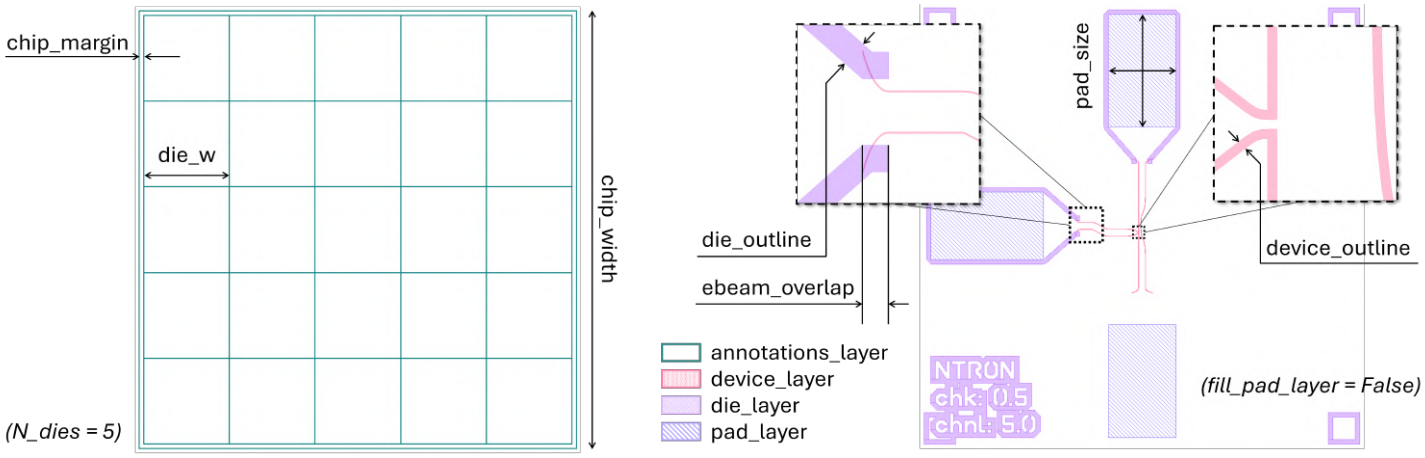
Previously in section 2.3.3, we went through the useful tools available in qnngds to build new cells from circuits. In this section, we will discuss the functions available for organizing these cells into a final design.

Design(): First of all, the class `Design()` regroups all parameters proper to the layout. Some of those parameters are proper to the die, as schematized in figure 16(a), and some of them will be shared throughout all cells of the design, see figure 16(b).

- **name** (str) – The name of the design.
- **chip_w** (int or float) – The overall width of the chip.
- **chip_margin** (int or float) – The width of the outline of the chip where no device should be placed.
- **N_dies** (int) – Number of dies/units to be placed by row and column.
- ***die_w** (int or float, optional) – Width of a unit die/cell in the design (the output device will be an integer number of unit cells).
- ***pad_size** (tuple of int or float) – Dimensions of the die's pads (width, height).
- ***device_outline** (int or float) – The width of the device's outline.
- ***die_outline** (int or float) – The width of the pads outline.
- ***ebeam_overlap** (int or float) – Extra length of the routes above the die's ports to assure alignment with the device (useful for ebeam lithography).
- **annotation_layer** (int) – The layer where to put the annotations.
- **device_layer** (int or array-like[2]) – The layer where the device is placed. (Usually corresponds to the layer for the low current e-beam exposure.)
- ***die_layer** (int or array-like[2]) – The layer where the die is placed. (Usually corresponds to the layer for the high current e-beam exposure.)
- ***pad_layer** (int or array-like[2]) – The layer where the pads are placed. (If used, usually corresponds to the final layer of metal for contact pads or heaters/resistors.)
- ***fill_pad_layer** (bool) – If True, the space reserved for pads in the die_cell is filled in pad's layer. (Useful when the pad layer and the superconducting layer are separated by an isolation layer. The "ground" will be accessible throughout the entire metal layer instead of on the ground pads only.)

At its `__init__()`, the `Design()` class creates a `DieParameters()` object that contains the parameters proper to the cells, marked with * in the list above. Even for special cases, all cells of a same layout share these parameters, hence even if they are proper to cells it makes sense to ask for them once at the design's creation instead of at every cell's creation.

create_chip(): After the parameters are chosen and the Design is initialized, the function `create_chip()` can be used not only to create a frame of the chip in the annotations layer (shown in figure 16(a)) but also to initialize a map (2D array) to monitor the placement of cells on the chip grid. Additionally, a text file keeping the cells coordinate along with their name is created if `create_devices_map_txt` is set to True.

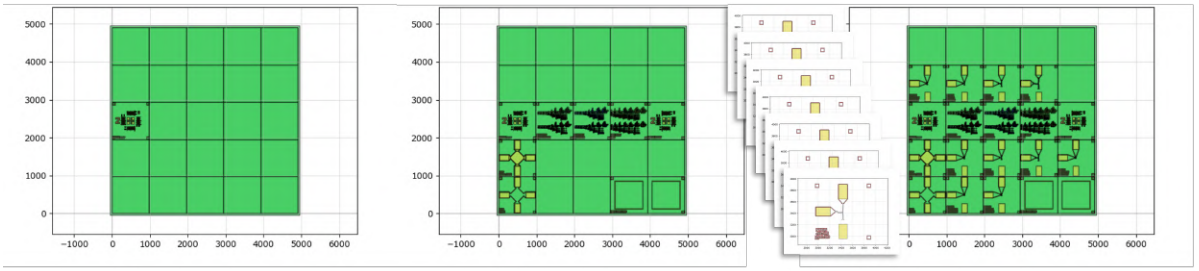


(a) (b)

Figure 16: The parameters of the `Design()` class, (a) concerning the chip, (b) concerning the cells.

place_on_chip(): This function is used to place a cell at given coordinates on the chip. Indices from 0 to N_dies − 1 are given for horizontal and vertical positioning, the Device is placed and added to the chip and a Warning is generated if a Device falls out of the chip or on an occupied place. If a devices map was created, the text file is updated with the new device added, as shown in figure 17.

place_remaining_devices(): This function acts as `place_on_chip()` except that the user does not specify position to place the cells. It can be useful when testing many small cells. First, the user should place the cells with critical positioning wherever they need them to be, then send to this function a list of cells to be positioned where there is available place, as shown in figure 17.



Devices placed on the chip:

(row, col) : device.name

(0, 2) : CELL.ALIGN(LEFT)

Devices placed on the chip:

(row, col) : device.name

(0, 2) : CELL.ALIGN(LEFT)
(4, 2) : CELL.ALIGN(RIGHT)
(0, 0) : CELL.VDP(MGB2)
(0, 1) : CELL.VDP(PAD & MGB2)
(2, 2) : CELL.RESOLUTION_TEST(MGB2 FINE)
(1, 2) : CELL.RESOLUTION_TEST(MGB2 COARSE)
(3, 2) : CELL.RESOLUTION_TEST(PAD)
(3, 0) : CELL.ETCH_TEST(PAD)

Devices placed on the chip:

(row, col) : device.name

(0, 2) : CELL.ALIGN(LEFT)
(4, 2) : CELL.ALIGN(RIGHT)
(0, 0) : CELL.VDP(MGB2)
(0, 1) : CELL.VDP(PAD & MGB2)
(2, 2) : CELL.RESOLUTION_TEST(MGB2 FINE)
(1, 2) : CELL.RESOLUTION_TEST(MGB2 COARSE)
(3, 2) : CELL.RESOLUTION_TEST(PAD)
(3, 0) : CELL.ETCH_TEST(PAD)
(1, 0) : CELL.NTRON(chk: 0.025, chnl: 0.125)
(2, 0) : CELL.NTRON(chk: 0.05, chnl: 0.25)
(1, 1) : CELL.NTRON(chk: 0.1, chnl: 0.5)
(2, 1) : CELL.NTRON(chk: 0.25, chnl: 1.25)
(3, 1) : CELL.NTRON(chk: 0.5, chnl: 2.5)
(4, 1) : CELL.NTRON(chk: 0.025, chnl: 0.25)
(0, 3) : CELL.NTRON(chk: 0.05, chnl: 0.5)
(1, 3) : CELL.NTRON(chk: 0.1, chnl: 1.0)
(2, 3) : CELL.NTRON(chk: 0.25, chnl: 2.5)
(3, 3) : CELL.NTRON(chk: 0.5, chnl: 5.0)

Figure 17: The evolution of the layout of a chip after adding devices using `place_on_chip()` (left and center) and `place_remaining_devices()` on various nTron cells (right). At the bottom, the simultaneous evolution of the `devices_map.txt` file.

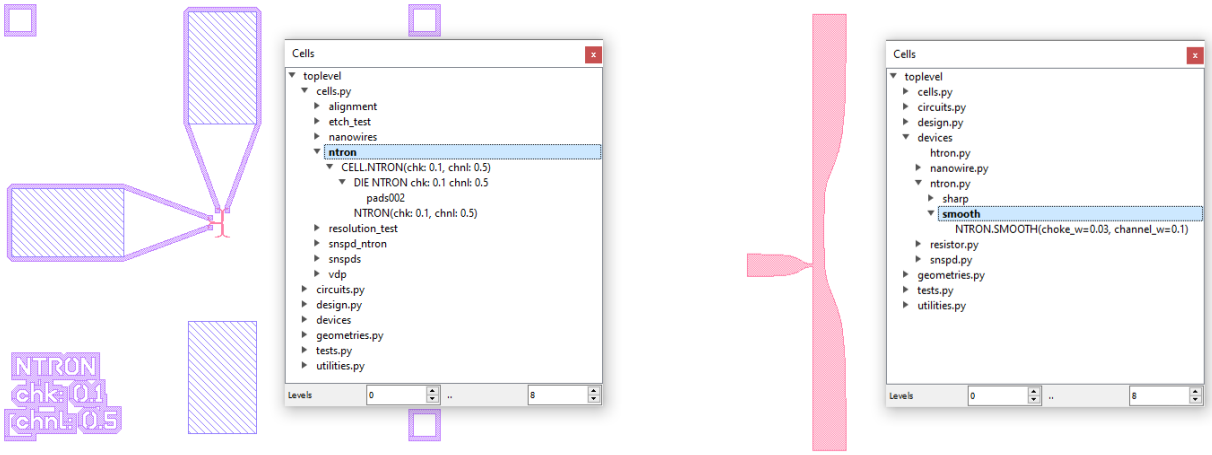
2.3.5 Contribute

Because qnngds is at its early stage, the library available is quite limited and a lot is yet to be done. Any user building a new layout using qnngds will by default code while respecting the structure of the package, meaning that contributing to it should not be too time consuming. Let's consider as an example that one has a new circuit to build.

- First, this circuit might be made of existing devices like `ntron.smooth()` or `snspd.vertical()` but it may as well require new devices that are not yet available like a smooth hTron for example. The new function can be added to `qnngds.devices.htron` module and named `smooth()`.
- Once all devices are available, the circuit can be built and contributed similarly to `qnngds.circuits` module.
- When integrating the circuit in the layout, if the user follows the proposed structure of cells for their layout, a cell will need to be created, as described in section 2.3.3. This new cell as well can be part of the library in `qnngds.cells`.

On the coding aspect, a complete documentation on How to contribute has been made as well and can be consulted for support.

In order to help contributing to the package, some tests are available and can be run to verify that the new contribution integrates properly. Running the test `all_dev_on_gds.py` will generate a gds file containing every device of the library. All devices, generated with their default parameters, can therefore be visualized and their structure studied, as shown in figure 18.



(a) (b)

Figure 18: The gds file obtained after running the test `all_dev_on_gds.py`. All functions of the package are displayed in the tree of cells. The ones returning Device objects have them added in the gds with their default parameters. Examples of (a) `cells.ntron()` and (b) `devices.ntron.smooth()`.

If a specific function needs to be tested, the simple test `single_dev_on_gds.py` can be used. In this case, the parameters don't have to be the default ones. This test is useful when creating a new device/circuit/cell. As the other test, it helps to visualize the hierarchy of the device created and if all elements are named.

After each contribution, the documentation needs to be updated. A single file (`generate_api.py`) has to be executed in order to automatically generate the new API (.rst) file. It also automatically plot and save the Device returned by the functions with their default parameters, and integrate them in the API. Qnngds is based on a Continuous Integration

Continuous Deployment approach. Each time a new branch of the repository is created and pushed, a new version of the documentation is created and compiled as well, under the name of the branch. It allows the contributors to verify that the new documentation displays properly before making the pull request.

2.4 How it can be further improved

As explained previously in this section, the current version of qnngds is the basis of a library for nanowire electronics to be completed. A list of issues have been created on the GitHub page with ideas and notes on corrections/contributions to bring to the package. Below are listed some ideas for the future development of the package:

- Associate classes of the design module to processes.
- Make classes inherit from others. Link `DieParameters()` and `Design()` more explicitly.
- Automate at maximum the integration of new devices in the package. Instead of having to do everything from the circuit to the cell's design, having functions like `make_cell()`.
- Even a graphic interface could be made once the package is solid.

For any development issue, a small documentation is also available and gives useful information relative to more in depth modification of the package, concerning the documentation or the python package.

Finally, we cannot insist enough on the fact that this package will truly be powerful only once people/students of the group will have contributed to it.

3 Fabrication of nanowire electronics in magnesium diboride

3.1 Introduction

While the initial discovery of MgB_2 was accompanied by much excitement, that enthusiasm has mostly disappeared due to the lack of progress made in implementing MgB_2 in practical devices.[17] One of the main challenges hindering the implementation of MgB_2 in superconducting electronics is the difficulty in synthesizing wafer-scale thin films.[13] Once synthesized, the challenge of obtaining functional superconducting devices remains significant due to the difficulty in preventing the oxidation of MgB_2.

Recent advancements have shown promise in overcoming these obstacles. For instance, Sergey Cherednichenko et al. demonstrated the fabrication of low kinetic inductance superconducting MgB_2 nanowires with a relaxation time of 130 ps for single-photon detection applications. They achieved nanowires as narrow as 20 nm with a large aspect ratio ($L/w > 3000$) using e-beam lithography and Argon ion milling. The thin film was deposited on a SiC substrate using Hybrid Physical Chemical Vapor Deposition (HPCVD). [6] Charaev et al. later report single-photon detection at a 1.55 µm optical wavelength, with the same fabrication and film deposition techniques employed. [5]

Alternatively, Kim et al. showcased the fabrication of superconducting devices in a co-sputtered MgB_2 film. Their process highlighted the necessity of passivation due to MgB_2's tendency to decompose and oxidize when exposed to air and water [13]. They developed a tri-purpose titanium-gold bilayer that served as a passivation layer during fabrication, a hard mask, and electrical contact pads.

In this section, we will present our work on fabricating devices using sputtered MgB_2 on a Si substrate, provided by the Jet Propulsion Laboratory. We will describe the efforts made to prevent film oxidation during the fabrication process and to achieve nanoscale resolution. Finally, we will suggest improvements for future work in the fabrication of MgB_2-based devices. Characterization of the fabricated devices can be found in the next section 4.

3.2 Process description

Before diving into the fabrication process description, we would like to mention that a process flow similar than the one presented by Kim et al. [13] has been tested on a first chip. We corrected the process as presented in this section after the failure of the e-beam exposure. Indeed, we considered the use of a gold hard mask for the process too constraining given our expertise on MgB_2 fabrication at the time.

In this section, we will detail the process steps required to achieve superconducting devices in Magnesium Diboride. The color boxes address various process-related questions that are crucial for ensuring good process control over repeated runs and provide potential solutions, notably in terms of test structures to add to the layout.

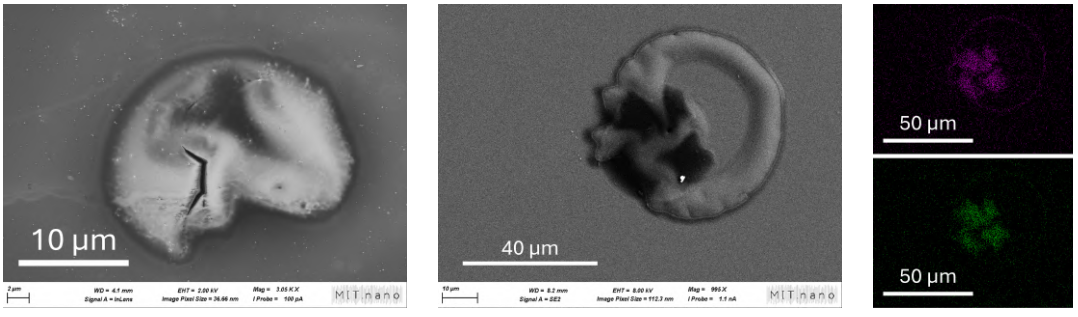
3.2.1 Depositing Magnesium Diboride

In this work, depositing MgB_2 was not one of our concern thanks to a collaboration with the Jet Propulsion Laboratory (California Institute of Technology, Pasadena, CA, USA) that provided us with one wafer. As schematized in figure 20.0, the wafer received is made from a commercially available Silicon substrate, on which was deposited 30nm of lowstress Silicon Nitride used as a buffer layer, 40nm of Magnesium Diboride and a capping layer of 30nm of Boron. MgB_2 was obtained after annealing its precursor Mg-B composite, deposited by RF magnetron sputtering. The Boron layer serves as an encapsulation layer and prevents magnesium evaporation during annealing. [13]

(Q0) Are there any visible defects on the sample? Of what kind?
Visual/Optical microscope/SEM inspection

At the reception of the wafer, some blobs like the ones shown in figure 19 were observed. These defects represent the first cause of failure of the process and we know from the start that some experiments/devices might not work depending on if they fall on a defect or not. Indeed, according to C. Kim (from JPL), the visible bubbles are regions of concentrated magnesium. These bubbles form, burst and undergo oxidation due to the high vapor pressure of magnesium.

We confirmed their says with SEM and EDS analysis of the blobs, as displayed in figure 19(b and c). Energy Dispersive Spectroscopy (EDS) identifies and quantifies elements on a sample by analyzing the energy of X-rays emitted after the sample is bombarded with an electron beam. We further confirmed, at the end of the fabrication, that the blobs or isolating by observing that the devices conduct as expecting when the blobs fall on the edge of a contact pad for example, i.e. the pad is still isolated from the ground surrounding it.



(a) (b) (c)

Figure 19: (a and b) SEM images of blobs on the sample. (c) EDS data of the blob in (b) for O (top) and C (bottom) elements.

After reception, the wafer was diced into pieces of 1cm x 1cm. The rest of the process is schematized in figure 20. Before starting the process, the piece was cleaned by sonicating it in acetone and rinsing in IPA.

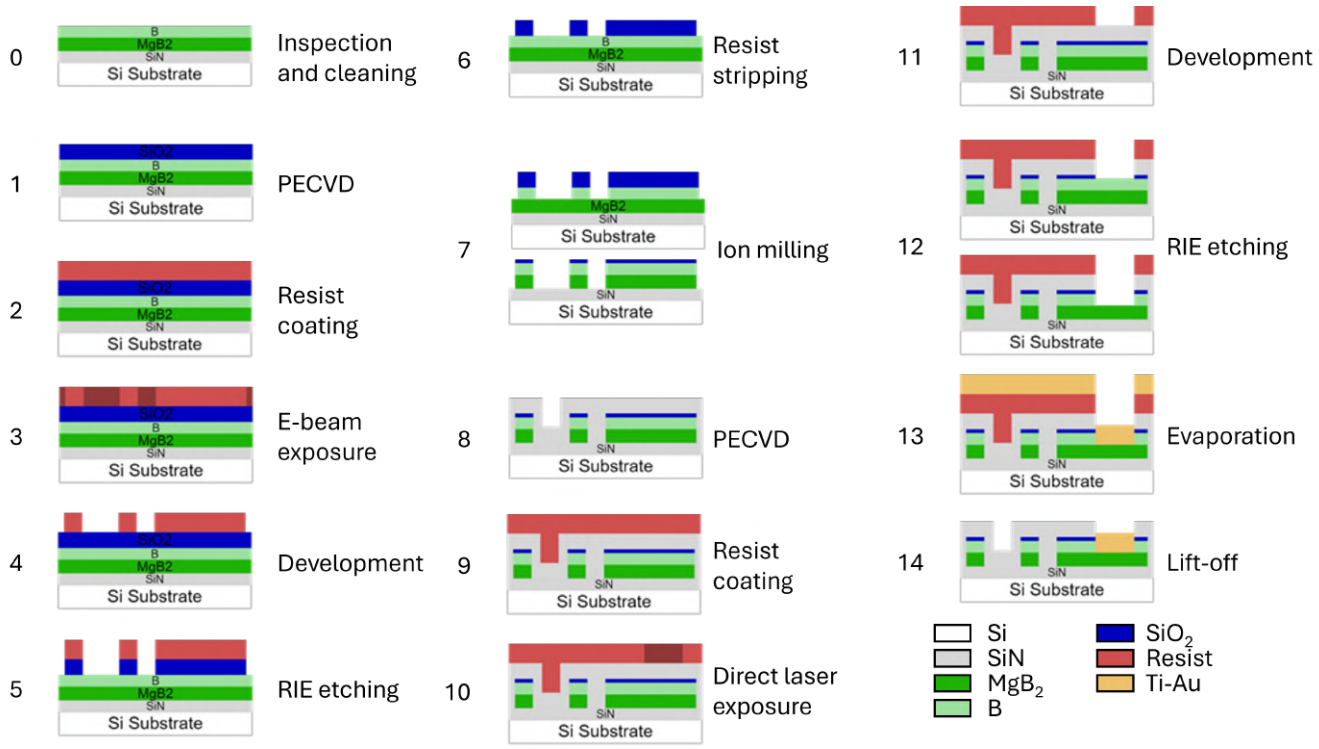


Figure 20: Schematic of the process flow employed.

3.2.2 Patterning the devices using e-beam lithography

Because MgB_2 oxidizes very easily, the main concern of the process is to avoid as much as possible to expose MgB_2 to air or oxidizing agents. Any resist developer or stripper would oxidize it, hence the etching of MgB_2 layer has to be made using a hard mask. 340nm of Silicon Dioxide has been deposited by PECVD, see figure 20.1. This thickness was determined based on the selectivity expected during the etching of 30nm of Boron and 40nm of MgB_2.

> **(Q1)** What is the actual thickness of the deposited SiO_2?
> *Optical measurement: spectroscopic ellipsometer or reflectometer.*

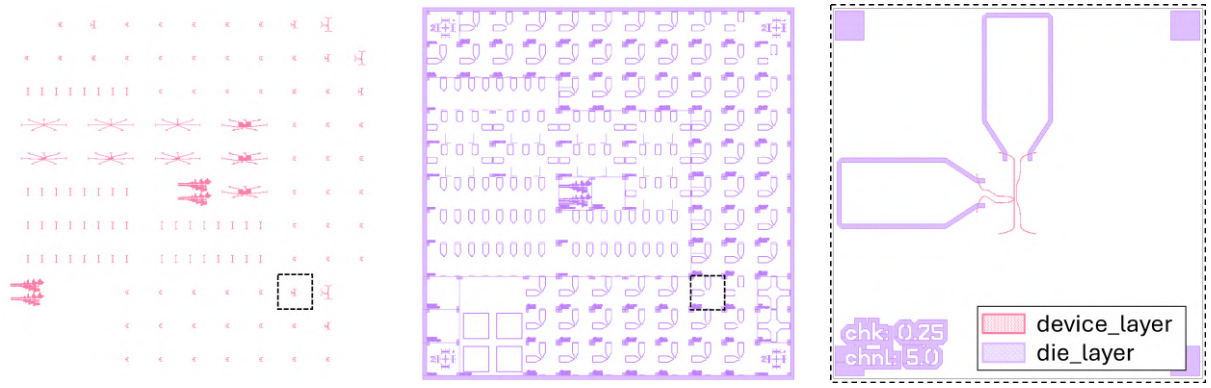
The layout will be transferred to this layer first, the resist stripped and only then the MgB_2 layer will be patterned. The e-beam lithography performed was relatively standard. ZEP530 was **spinned** at 3k rpm and baked for 2min at 180°C to obtain a thickness of about 440nm. Electra 92 was spinned as well at 2k rpm and baked for 1min at 90°C, for making the sample electrically conductive. The sample was attached to a conductive metal sample holder and a conductive grounding clamp linked the thin layer of conductive polymer deposited to the metal holder.

> **(Q2)** What is the actual thickness of the deposited resist?
> *Optical measurement: spectroscopic reflectometer*

After data conversion using BEAMER, also accounting for ebeam proximity effect correction

(PEC), the sample was **exposed** in a HS50 tool at 220µC/cm^2. In order to reach the finest resolution while limiting the exposure time, the smallest features (see figure 21 in pink) were exposed at 1nA while the largest features (see figure 21 in purple) were exposed at 10nA. The resist is **developed** for 60s in xylene at 5°C followed by 30s in IPA at room temperature.

(Q3) Are the two exposures (fine and coarse) well/sufficiently aligned?
Microscope inspection. Include alignment test structures between the fine and coarse layers.
(Q3.1) Is the pattern correctly transferred to the resist? What is the achieved resolution?
Image the resolution test structures with a SEM. Do prior dose tests to optimize the parameters of exposure.



(a) (b) (c)

Figure 21: The two layers to successively expose with e-beam at (a) low current for smallest features like devices and (b) high current for the biggest features like contact pads. (c) Zoom on one typical cell of the layout.

After the lithography, whose steps correspond to figure 20.2/3/4, the **hard mask** can be **etched** using Reactive Ion Etching (RIE) until the Boron layer. The process, corresponding to step 5 in figure 20, is again quite standard. The chemistry used was CF_4 and Ar. A sister chip was sent next to the sample in order to estimate roughly when the mask was etched through. 4+1 cycles of 30s were enough to open the mask. It also fully removed the resist and hence thinned the mask as well, leaving 130nm of SiO_2.

(Q4) Was the RIE selective enough and well timed not to etch through the boron layer?
Send in a sister chip without resist. Optical measurement: spectroscopic ellipsometer or reflectometer.
(Q5) Is the pattern well transposed to the SiO_2 layer (e.g. under-etch issue)? Did we lose in resolution? *Simple microscope inspection. For even more precision, image the resolution test structures with a SEM.*

The sample was rinsed in acetone and IPA after the etching, risking no oxidation since the boron layer is still protecting MgB_2.

(Q4.1) If the RIE etched through the boron layer, is MgB_2 oxidized (or altered)?
Use the sister chip to probe the resistivity of MgB_2.

Only then, the **pattern** can be **transferred to the MgB_2** layer. This step (schematized in figure 20.7) was finally done in an ICP-RIE tool, the recipe was taken from Emma's work (process parameters: 400W ICP / 300W bias / 1Pa pressure / 30sccm BCl_3 for 120s).

(Q6) Is MgB_2 fully etched through?
Send a sister chip. Probe immediately after the etching runs if the sample is still conducting (i.e. if there is MgB_2 left unetched).
(Q7) Is the pattern well transposed to the superconducting layer? Did we lose in resolution?
Start with a simple microscope inspection. For more precision, image the resolution test structures with a SEM.

Below is a brief description of the procedure required for typical critical etches like this one.

- Developing the recipe: what is the etch rate of B, MgB_2 and SiO_2? What is the best combination of parameters for the etch to be as selective as possible and the pattern to be transferred with high fidelity? (Obviously, if the test chips are not patterned, this last point will have to be omitted).
- At the beginning of any machine's operation, the chamber needs to be cleaned and conditioned. Indeed, the etch rates and reactions will be different depending on the chamber conditioning, for e.g. depending on which chemistry used the previous user of the machine.
- Just before the critical run, send pilot chips to determine the tendency of the etching in these conditions (even after the chamber conditioning). Adjust (or not) the time of the process based on the current SPC (Statistical Process Control) results.
- During the run, send in sister chips to have the real time and (almost) similar conditions than the sample of interest.

The glue used to hold the sample in place and thermally conduct the heat on the carrier wafer was removed as well as possible by carefully rubbing the back of the chip on a paper towel dampened with acetone, without putting in contact the top of the chip. This step underscores one of the challenges of working with rare and expensive materials: it necessitates the use of chips instead of wafers, which is not optimal in cleanrooms because the machines are designed for wafers, and manipulating chips is much more delicate than handling wafers.

3.2.3 Encapsulating and patterning contact pads

Immediately after the MgB_2 layer was patterned, the chip was placed under vacuum and an encapsulation layer of 80nm of Silicon Nitride was deposited by PECVD. Even if we believe that some of the Boron is left on top of the MgB_2 layer, the material could still oxidize from the sidewalls of the etched pattern. This is why the encapsulation layer is necessary. See section 3.3.1 for more details on how the MgB_2 was oxidized, most likely between the etching and the encapsulation steps; even if a short time only separated those two steps.

Once the sample is encapsulated, contact pads have to be added in order to electronically access the devices. For this, an additional lithography has to be performed. In order to avoid oxidizing MgB_2, the choice was made to use the same resist for etching the encapsulation layer and depositing the pad material with a lift-off process.

nLOF 2035 was **spinned** at 3k rpm for 60s and baked for 90s at 110°C. The pads layer was **aligned and exposed** used direct laser writing (on the MLA) with a dose of 300mJ/cm^2 using the 375nm laser. A post exposure bake was done for 90s at 110°C before the **development** for 90s in AZ726. (See figure 20.9/10/11.)

(Q8) Is the second lithography well aligned with the first one?
Microscope inspection, use alignment marks structures to get the error in alignment.

The Silicon Nitride and remaining Boron were etched through by dry etching using a SF_6 chemistry.

(Q9) Is there Boron remaining?
Electrical probing on any device. Necessitates the use of a probe station if the pads are not big enough for contacting with a multimeter. If included in the layout, use etch test structures.
(Q10) Is the top of the MgB_2 layer not altered?
Electrical probing, use Van der Pauw test structures to determine if the sheet resistivity has changed.

After the pads are opened, the Magnesium Diboride is exposed again to air and the evaporation of Titanium (10nm as adhesion layer) and Gold (60nm) has to be done immediately. Finally, the resist is lifted-off in acetone over several hours.

(Q11) Is the resist well lifted?
Visual/Microscope inspection.

3.3 Process discussion

3.3.1 Alteration of Magnesium Diboride film during the process

The most evident aspect of the process flow to be discussed is the superconducting film quality. After the process, we measured its critical temperature on several devices. A schematic of the electrical setup used to take the measurement is shown in figure 37. A current is continuously sent to a patterned nanowire and the voltage across the device is measured while the temperature is swept from 7K to 50K. One example of the result obtained is given in figure 22. The one result given here concerns a measurement made on a nanowire shaped as a simple constriction of width 0.5µm. The critical temperature measured is around 24.5K.

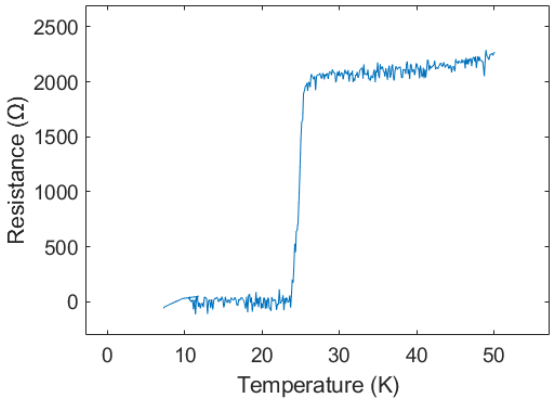
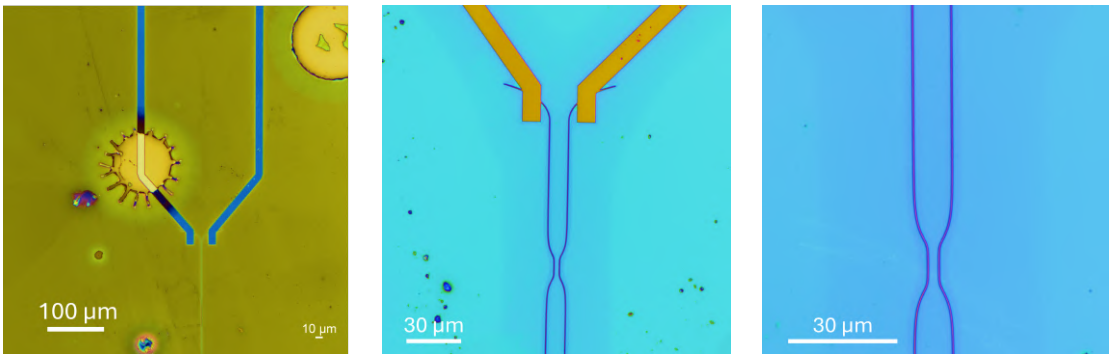


Figure 22: Critical temperature measurement of a device after the fabrication process is completed. The one result given here concerns a measurement made on a nanowire shaped as a simple constriction of width 0.5µm. The critical temperature measured is around 24.5K.

As delivered from JPL, MgB_2 film had a critical temperature of 37.5 K. After the process,

the critical temperature was down to 22-26K depending on the devices. This is an indication of the film's alteration during the process.

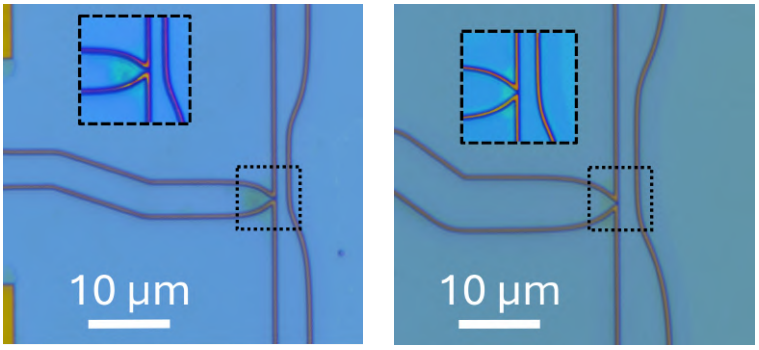
Several causes of degradation could be responsible for this difference, the main one is the oxidation of Magnesium Diboride, particularly between steps 7 and 8 (see figure 20). Microscope images taken at the end of the process reveal a change in color surrounding the etch pattern, most probably being the beginning of MgB_2 oxidation. Figure 23(a), taken right after MgB_2 etch, might show a very slight lighter color around the edges of the pattern but the "oxidation" is unclear. However, the image in (b), taken after the encapsulation (hence after several more minutes exposed to air before being encapsulated in SiN), clearly shows a shadow around the edges of the pattern, indicating the material was altered. Figure 23(c), taken at the end of the process (around 3 weeks after figure (b)), reveals no difference with (b), confirming that the encapsulation is efficient.



(a) (b) (c)

Figure 23: Microscope images, with increased saturation, of some devices (a) right after MgB_2 etch, (b) after the encapsulation (several more minutes exposed to air than (a)), (c) the same device than in (b) but 3 weeks later.

In addition to seeing these shadows, most probably due to oxidation, weird effects have been observed and particularly concerning the nTrons' gates. After the process, none of the nTrons' gates was conductive, even the ones that had the same dimensions than simple constrictions. Indeed, in figure 24 showing images taken under a microscope of nTrons and a zoom on their gate, intense difference of color is observed at the gate of the nTrons.

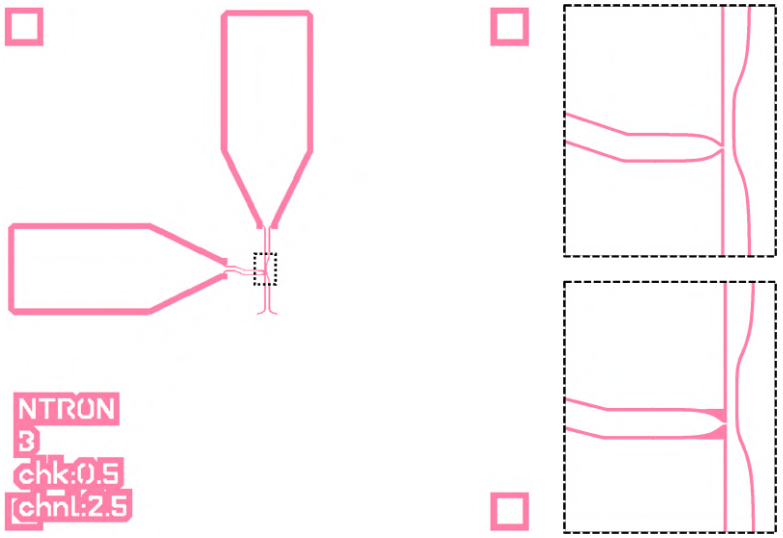


$w_{gate} = 0.25\mu m$
$w_{drain} = 1.25\mu m$
(a)

$w_{gate} = 0.1\mu m$
$w_{drain} = 2.0\mu m$
(b)

Figure 24: Microscope images of several nTrons taken at the end of the process. Insets are high saturated zooms on the gates of the nTrons.

The main hypothesis behind this observation is that charging effects influenced the plasma concentration and distribution during the etching. One easy way to verify this hypothesis would be to pattern the same layout using ion beam etching instead, a dry etching process where the plasma is separated from the sample, and the ions are accelerated through optical grids to create a beam, often using an inert gas like Argon to bombard the sample. Another way to verify this hypothesis would be to use the same etching process but adjust the layout instead, removing potential sharp regions electrically connected, as shown in figure 25.



(a) (b)

Figure 25: Example of how to correct the layout in order to verify the hypothesis of charging effect during the MgB_2 etch. (a) Example of a nTron cell. (b) Zooms on the layout: (top) without correction, as exposed in the fabrication run described, (bottom) after correction to avoid the charging effect.

Other discrepancies as the ones shown in figure 26 rather illogical or for the less hard to explain are observed on the chip and confirm that the process is still to be improved. In this example, the gate and drain had at room temperature a resistance of 127Ω and $1.33k\Omega$ respectively but appeared shorted after cooling doing the chip below the superconducting critical temperature.

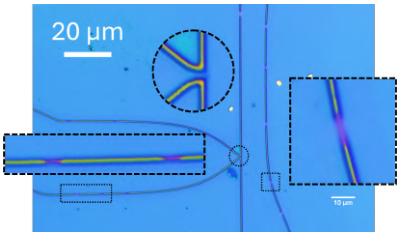


Figure 26: Zooms on discrepancies in the etching lines of this device. This image was modified to increase the saturation of colors.

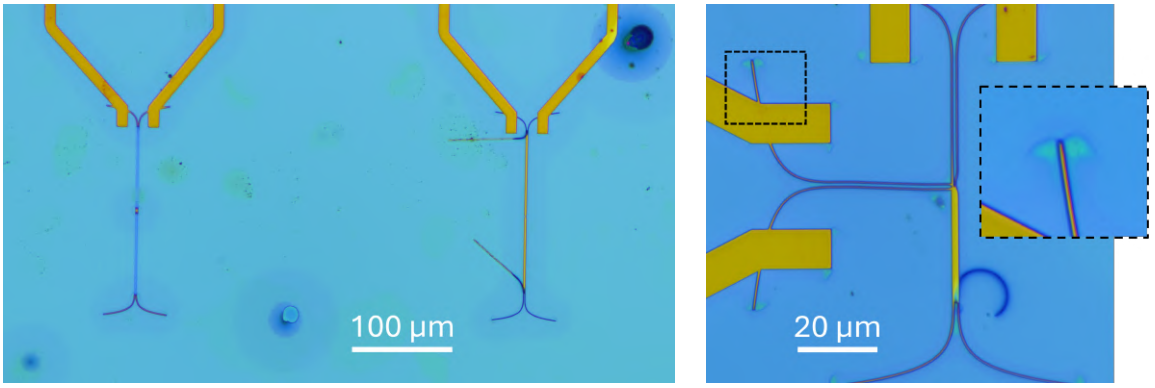
3.3.2 Films stress mismatch

Another concern during the fabrication is the films stress mismatch. Several regions could be of concern and are listed below:

1. The 40nm layer of MgB_2 on 30nm SiN and its 30nm Boron capping layer above it.
2. The e-beam resist ZEP350 adhesion on the hard mask of SiO_2.
3. The hard mask of SiO_2 on the Boron layer.
4. The encapsulation with SiN.

Until the etching through MgB_2, no issue relative to films stress was observed. After this step, some of the narrowest traces delaminated. We had very few time to image the chip between the etching and the encapsulation in PECVD to avoid oxidation, introducing some unknown in

the origin of the delamination observed after the encapsulation, see figure 27. In these pictures it is clear that the yellow color corresponds to a stack the Silicon substrate with SiN on top (similar to the pads outline). However, what is unclear is when the delamination occurred. Did the delamination appeared during the etching of MgB_2, i.e. are the delaminated wires a stack of $MgB_2/B/SiO_2$, B/SiO_2 or SiO_2? Or did the delamination appeared during the encapsulation in SiN, i.e. are the delaminated wires a stack of $MgB_2/B/SiO_2/SiN$? Other elements like the one highlighted in figure 27(b) appear like cracks, again with high uncertainty on where or when they appeared. The one observation that might be worth noting is that the "oxidation shadow" follows those cracks as well.



(a) (b)

Figure 27: Microscope images (at higher saturation) of delaminated devices taken after the encapsulation in SiN.

3.3.3 Improving the process control and monitoring

The etching processes involved were highly intricate and posed significant challenges. Each step requires precise control to achieve the desired outcomes without compromising the integrity of the materials involved. The first improvement would be to have a better control on the etching processes, by developing recipes with high selectivity and consistent etch rates.

The second focus would be on monitoring the etching: having tests to perform in order to determine the state of the chip before, during and after the etching. Given that these devices are fabricated on chips, conventional endpoint detection systems are likely ineffective due to the insufficient signal from the small structures. Optical endpoint detection is impractical because the structures are too small, and while ion mass spectroscopy might provide adequate results for wafers, it is not suitable for these chip-based devices. The use of pilot and sister chips is one way to go around this challenge. However, we were mainly limited after the etching to electrical probing and visual inspection on those chips as the MgB_2 model used currently for ellispometry and interferometry is not always accurate.

Direct inspection and probing on test structures on the chip is another way to monitor the process. For processing Magnesium Diboride though, the question of oxidation always dominates over letting the chip for even half an hour exposed to air for testing. One interesting study to further perform would be focusing on how and how fast Magnesium Diboride oxidizes, as well as how to characterize the oxidation.

A second fabrication run, incorporating some of the discussed improvements, was performed by Emma. Although the details of this run are not covered here, as it falls outside the scope of my work, we anticipate that the outcomes will provide further insights into MgB_2 processing.

4 Characterization of fabricated devices

4.1 Introduction

The advancement of nanowire electronics and superconducting nanowire single-photon detectors (SNSPDs) has revolutionized various technological domains like quantum computing, medical imaging, and astronomical observations. Central to these innovations is the quest for materials that offer superior performance characteristics, particularly in terms of superconductivity.

Among the materials under investigation, Magnesium Diboride emerges as a particularly promising candidate, mainly because of it's remarkably high critical temperature of 39K [18]. Difficulty of deposition in uniform and low roughness thin films for superconducting nanowires applications, and the material instability, still makes MgB_2 a rare and uncommonly used material in these application, despite the abundance of its constituent elements in nature. Consequently, gathering material properties and post-processed characteristics of MgB_2 thin films is of huge interest.

Proper characterization of nanowires is an essential first step toward developing larger superconducting devices and circuits, as well as more advanced technologies such as single-photon detection. From simple IV curves to the analysis of switching current distributions, there is still much to learn about the material properties of MgB_2 and, more importantly, the physical mechanisms involved in switching a nanowire from its superconducting to normal state.

The understanding of the switching mechanism in nanowires is still limited, especially regarding the physical reasons for fluctuation phenomena or dark counts. There is a lack of a comprehensive physical model to predict and explain the switching mechanism of superconducting nanowires. Therefore, any analysis that contributes to this phenomenological understanding is highly valuable.

In this section, we will go through the first rough characterisation of our MgB_2 fabricated devices using a cryogenic probe station first and then a cryostat (freespace). In a second time, we will describe how we performed the analysis of the switching current distributions in various nanowires and discuss the results obtained.

Note that all results displayed here concern the 40nm-thick MgB_2 chip (ID: JMB021), whose fabrication process was described in the previous section.

4.2 Literature review

This literature review will focus on the analysis of switching current distributions in superconducting nanowires. Two studies were the main foundation of this work:

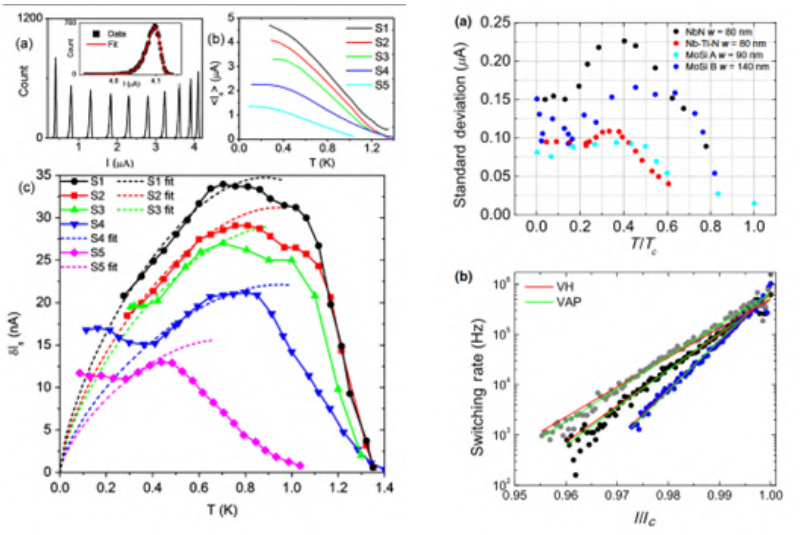
- Salvoni et al., "Activation Energies in Mo Si / Al Superconducting Nanowire Single-Photon Detectors.", 2022.
- Li et al., "Switching Currents Limited by Single Phase Slips in One-Dimensional Superconducting Al Nanowires.", 2011.

The main idea behind such studies is to match theoretical models to experimental data. The complexity of the models require more than the mean switching current of the nanowires for comparisons, justifying the need for the analysis of their histograms.

Histograms gathering the switching current of thousands of sweeps for several temperatures are recorded on nanowires. Depending on the nanowires dimensions and the temperature range considered, some mechanisms can be excluded or considered as responsible for the fluctuation rates.

(Salvoni et al. 2022) measurements are performed on nanowires selected to respect the relations $d \leq \xi \ll w$ and $4.4\xi \leq w$ respectively assuring that the system can be considered quasi two-dimensional and that nucleation and vortices propagation can occur, ξ being the coherence length. They focus on vortices models: the unbinding of vortex-antivortex pairs (VAP) and vortices hopping (VH) mechanisms.

(Li et al. 2011) mention the nanowires lengths l to be in the range of $15\xi_0$ to $100\xi_0$ and width w to be roughly $1/10\xi_0$. They focus on phase slips mechanisms and particularly on thermally activated single phase slip (TAPS) in a range of temperature from $\sim 0.3\,\mathrm{T_C}$ to $0.6\,\mathrm{T_C}$.



(a) (b)

Figure 28: Extracted figures from (a) Salvoni et al. 2022 and (b) Li et al. 2011. This figure highlights that from simple histograms recordings (top left) can be obtained the mean switching current vs temperature, the standard deviation vs temperature and the switching rate versus bias current; and that from these data can be modelled, compared and fitted physical mechanisms responsible for the nanowires fluctuation phenomena.

Models representing physical explanations for the switching mechanism are fitted to the acquired data. Depending on the study, either the standard deviation or the switching rate were used as the basis for the fits; see figure 28 (a) for switching rate and (b) for standard deviation. Note that the switching rate is obtained from the bins and counts of the recorded histograms by applying the Kurkijärvi-Fulton-Dunkleberger transformation [8].

In any case, when the overcoming of the energy barrier is due to thermal excitation, the rate of dissipative events, which are referred to as fluctuations, can be expressed through the Boltzmann factor, as shown in equation 3. It is $U(I_b, T)$ analytical expression only that differs depending on the fluctuation phenomena considered.

$$\Gamma(I_b, T) = \Omega \exp\left(-\frac{U(I_b, T)}{k_B T}\right) \tag{3}$$

4.3 First measurements

The goal of the firsts measurements performed was simply to get an idea of the main characteristics of the devices: critical current density, critical temperature or even simply determine if some devices are superconducting.

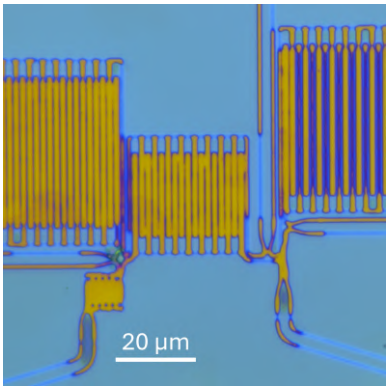


Figure 29: Picture of a non-operational circuit imaged under an optical microscope.

The characterization starts by imaging the devices. Using an optical microscope allowed us to exclude many devices that were not worth measuring (see the previous section in figure 27 for example or figure 29). Because of the 80nm of SiN encapsulation to prevent MgB_2's oxidation, the pattern is not (or hardly) visible with Scanning Electron Microscopy (SEM), even at high accelerating voltage (30kV). This first visual inspection of the chip state leaves us with the map of devices to test given in figure 30.

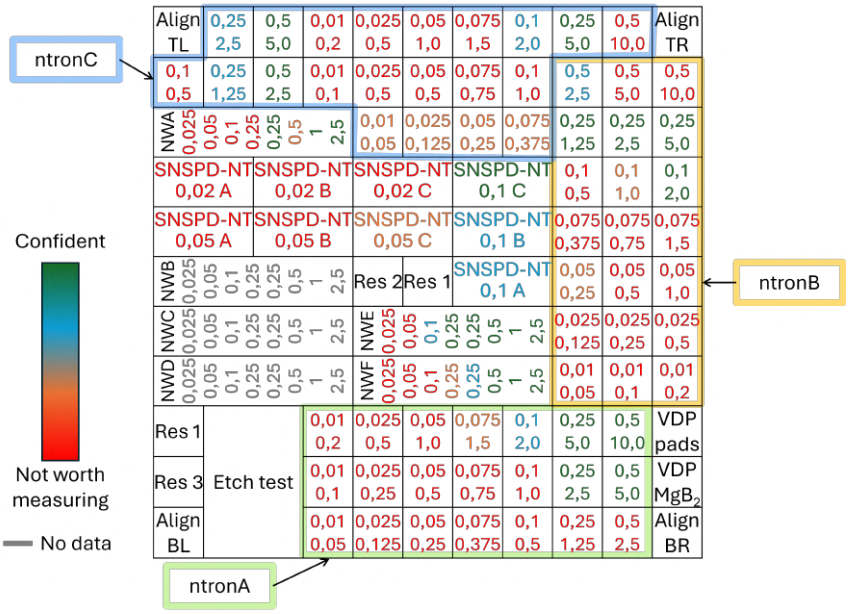


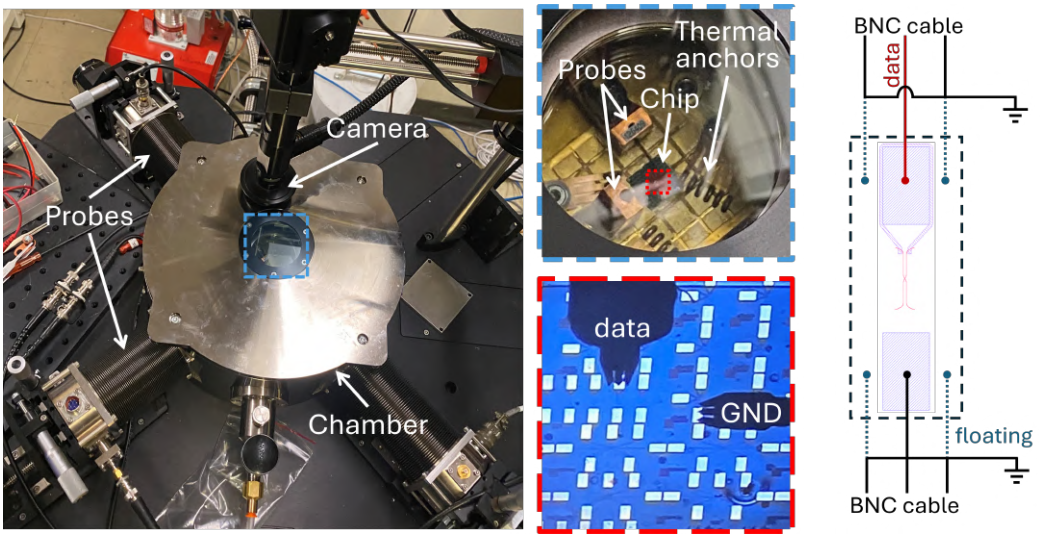
Figure 30: Schematic of the chip cells and their defined IDs. The experiments are color-coded based on the confidence level, derived from optical inspection, indicating the likelihood of success.

We will present in this section some devices that were superconducting. Let us simply mention that no nTron's measurement will be presented here, as all gates were disconnected, even though they did not appear open and some nanowires with similar critical dimension were superconducting. See section 3.3.1 and figure 24 for more discussion on this subject.

4.3.1 First measurements in Lake Shore probe station

The first tests were done in a cryogenic probe station, imaged in figure 31(a). It has the advantage of not requiring wire bonding the devices, which is ideal to quickly determine which one are superconducting. Indeed, the other cryostats of the lab that we could use have a limited number of electrical lines, implying that they need to be warmed up and cooled down again every time lines need to be switched to other devices.

With the probe station, equipped of 2 GSG-probes, we were able to test simple nanowires (one probe for the data, the other one for the ground) since the patterned superconducting layer is encapsulated and accessible only through contact pads, i.e. the ground is not filled in the metal layer, see figure 31(b). That is something that have been corrected as well in the new layout for the second fabrication run (option fill_pad_layer in qnngds).



(a) (b)

Figure 31: (a) The probe station, with detailed views of the sample stage and the chip during a measurement. Note that all grounds are shared among the devices in the chip design, which explains the probe configuration on the chip. (b) A schematic showing the use of GDG probes for measuring our nanowires, where the ground is accessible only through contact pads.

Several nanowires have been probed following the setup schematized in figure 32. For each device, the critical current is theoretically restricted by its width since the temperature of the sample is supposed to be constant as well as the thickness of the MgB_2 layer.

The way the measurements are typically done is by first sweeping the current through a large range to be certain of switching the device to its resistive state, and then take a new measure ramping the current until a point close to the switching current of the device in order to avoid heating effect as much as possible. Note that the current is converted by using a resistance through a voltage source (Yokogawa GS200). The higher the resistance R_S, the lower is the noise of the current I_S. However sometimes, we are forced to use a lower resistance because the switching current is too high for the 30V limitation of the voltage source used. The voltage accross the nanowire is then recorded through a multimeter (Keithley 2400). As an example, in order to obtain the IV curve of a 1 μm large nanowire, the source current was swept to 1 mA. The resistance R_S chosen was of 10 kΩ, implying the source voltage V_S to be swept to 10 V.

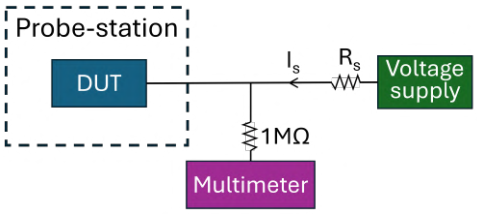


Figure 32: Electrical diagram of the setup for measuring IV characteristics of devices in the probe-station. *Note that the lines represent BNC cables.*

A typical IV curve obtained is given in figure 33. It is composed of several parts:

- A vertical line centered at 0 V, being the range of currents, for a fixed temperature, at which the device is **superconducting**.
- The red cross is the point at which the nanowire switches from its superconducting to its normal state. The corresponding current is called the **switching current**. It is related to the switching current density by the formula: $J_{sw} = I_{sw}/(w \times t)$ where w and t are the nanowire width and thickness respectively.
- The blue cross is the point at which the nanowire switches back from its normal to its superconductive state. The corresponding current is called the **retrapping current**.
- In our case, we expect the positive and negative parts of the IV curve to be symmetric, but we can similarly define the (negative) switching and (negative) retrapping currents.

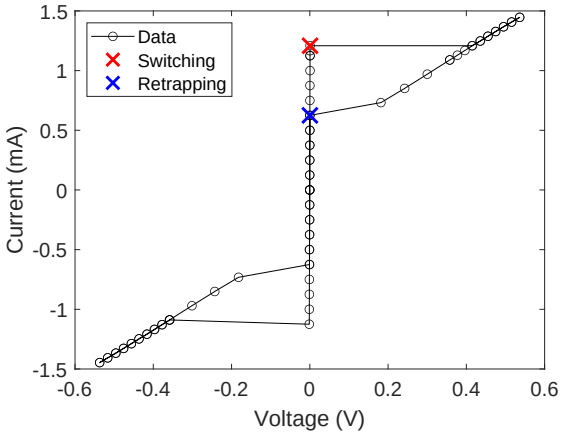
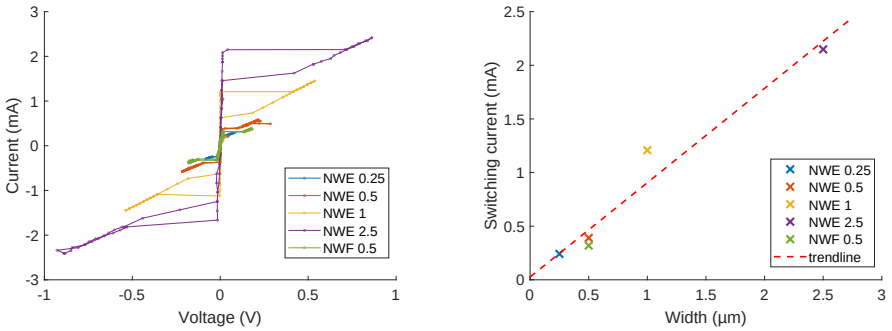


Figure 33: Typical IV curve obtained. The device is a simple constriction of 1 µm width. The measurement was done in the probe-station, at an estimated temperature of 9 K. The switching and retrapping currents are respectively evaluated at 1.2 mA and 0.6 mA.

After measuring IV curves on multiple nanowires, we can plot the switching current of devices with respect to their width, as shown in figure 34. The relation obtained can be linearly fitted by the equation $I_{sw} = 0.88w + 0.03$ leading to $J_{sw} \approx 22\,\mathrm{mA\,\mu m^{-2}} \approx 2.2\,\mathrm{MA\,cm^{-2}}$. Keeping in mind that this switching current density value refers specifically to our 40 nm thick processed MgB_2 layer at the temperature of the sample in the probe station, roughly estimated at 9 K.



(a) (b)

Figure 34: (a) IV curves obtained for several constrictions. (b) Corresponding switching current with respect to their width. The trend-line equation is $I_{sw}(mA) = 0.88 \times w(\mu m) + 0.03$.

Even if we were able to extract some interesting and promising results out of the few devices tested with the probe station, we needed to move the measurements to a different cryostat to have a good control on the temperature, and wire-bond the experiments for precise and consistent measurements.

4.3.2 Second measurements in the freespace, varying the temperature

After having performed measurements in the probe station, we started to characterize some devices in the "freespace", a cryostat able to cool down to about 3.6K (before its update, at the end of my visit in the group) and that has heaters on the sample stage, allowing for a better control of the temperature during the measurements. The freespace has the advantage over other tools to cool down the sample without putting it in contact with liquid helium, that might oxidize Magnesium Diboride in case of bad encapsulation. The drawback is that the number of connections is limited to 6 RF lines.

In this section, we will focus on 3 different runs performed in the freespace. We will first briefly discuss the procedure from the chip to its cool down. Then, we will talk about what measurements were performed and how. Finally, we will discuss the results.

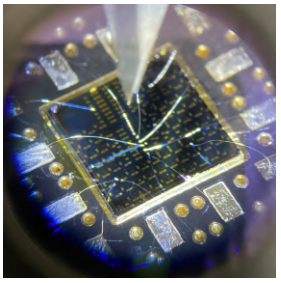
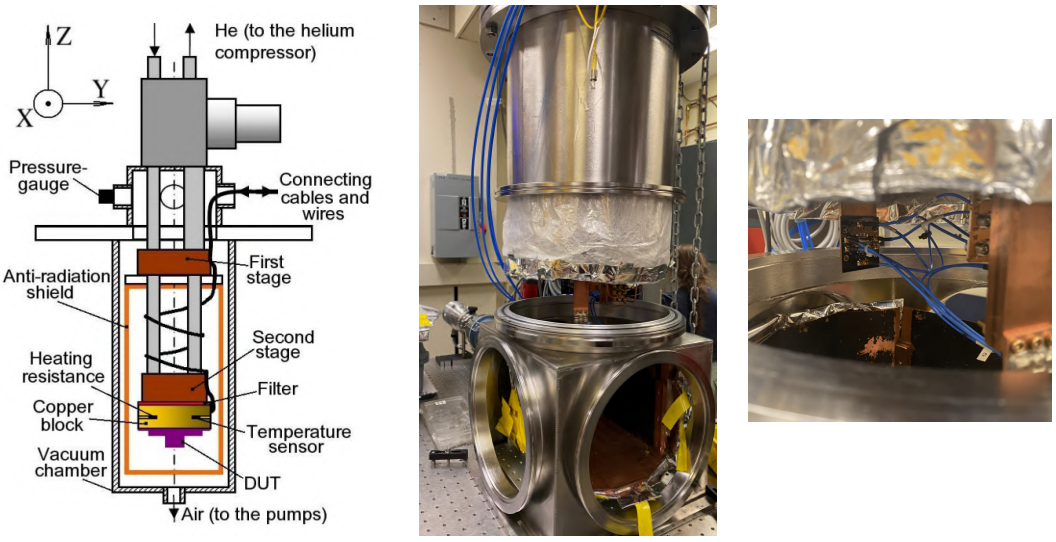


Figure 35: Picture of the chip wire-bonded to the PCB.

First, the chip is assembled onto a PCB, interfered with a viscous paste (GE Varnish) for cryogenic heatsinking. The devices to probe are wire bonded to the PCB's pads (see figure 35) and we verify that they are electrically connected by measuring their resistance through the PCB's connectors. Note that some precautions need to be taken to avoid electrostatic discharge (ESD) damage while wire bonding: wrist straps and footwear are used for personal grounding, ESD mats are placed on the workstation and last but not least the bonding starts by connecting the grounds and then the data lines.

Once the PCB is assembled, it is ready to be cooled down. In our case, the cryostat used is quite similar to the one schematized in figure 36(a). The procedure for cooling down the freespace is relatively simple:

1. Evenly spread vacuum grease on the back of the PCB using a spatula.
2. Screw the PCB to the sample stage.
3. Connect the PCB's ports to the RF lines in the chamber and write down the equivalences.
4. Finish the assembly by contacting the top and bottom part of the instrument, connecting the thermal braid, and closing the thermal and anti-radiation shields.
5. Seal the vacuum chamber and turn the rough pump on. Wait for the pressure to go down to at least 10^{-2} Torr.
6. Turn on the turbo pump. Wait for the pressure to go down to at least 10^{-4} Torr.
7. Start the compressor. The temperature should go down to at least 4 K.



(a) (b) (c)

Figure 36: (a) Schematic view of a typical cryocooler.[9] (b) Picture of the freespace when opened to access the sample. (c) Focus on the PCB attached to the sample stage and connected to the RF cables.

The objective of the following measurements was to have a global idea of the behaviour of the switching current of devices with respect to temperature. For this purpose, we used the setup schematized in figure 37. The temperature was manually increased and, similarly than described previously in section 4.3.1, the IV curves of several devices were recorded. The constrictions probed and presented in this section are summarized in table 1. As mentioned previously, some nTrons were tested as well, without success, see table 3 in the Appendix.

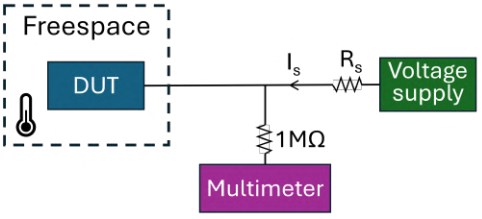


Figure 37: Electrical diagram of the setup for measuring IV characteristics of devices at various temperatures in the freespace. *Note that the lines represent BNC cables.*

Run	**ID**	**Width**	**Status**
(1)	NWE 0.1	0.1 µm	resistive
(1)	NWE 0.5	0.5 µm	SC
(1)	NWE 0.25-10	0.25 µm	SC
(3)	NWE 0.5	0.5 µm	SC
(3)	NWE 2.5	2.5 µm	SC

Table 1: Constrictions tested in the freespace. Note that some devices have been tested at multiple runs (cool down).

Figure 38 gives the IV curves of three different constrictions of width 0.25 µm, 0.5 µm, and 0.5 µm at temperatures from 4 K to 30 K. Such graphs are typically the sign of superconductivity,

as explained previously. The IV curve obtained for NWE 0.1 is given in figure 51 of the Appendix, found to be resistive.

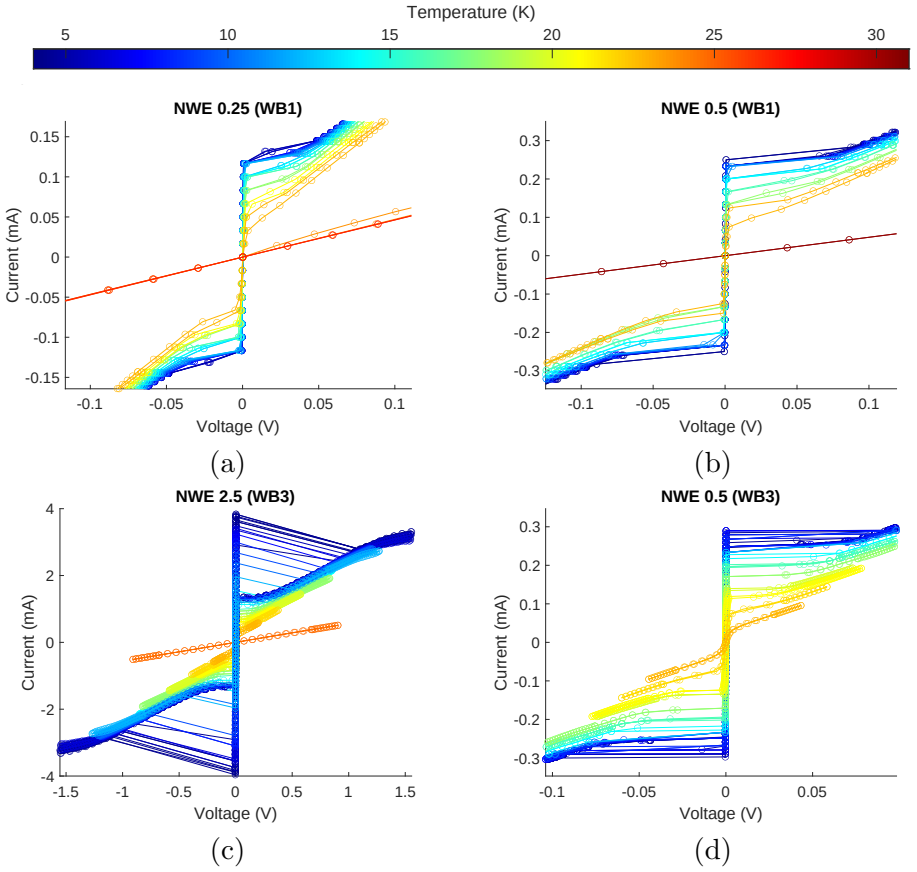


Figure 38: IV curves of several constrictions of width (a) 0.25 µm, (b) 0.5 µm, (c) 0.5 µm, (d) 2.5 µm at temperatures from 4 K to 30 K

The switching current was defined in the code as the current corresponding to the maximum differential voltage between two consecutive measures, in the first quarter of the sweep (i.e. positive current, positive sweep).

Figure 39 (figure 40) show plots of the switching current (density) vs temperature obtained from the IV curves. We can distinguish some plateaus in the switching currents for consecutive temperatures. This effect is directly linked to the number of measurements taken for a sweep and the way the switching current is extracted here. This is not a physical property of the devices.

We further observe that NWE 0.5, measured at two different runs on April 10th (figure 39(b)) and on May 14th (figure 39(c)), produced similar results. Although this does not constitute a rigorous proof, it suggests that the devices are likely to remain stable over time and under fatigue. The data were experimentally fitted to obtain the equations shown in the graphs legend, except for NWE 2.5 (in figure 39(c)) for which no good fit was found.

Theoretically, if the alteration of the MgB_2 layer during fabrication is independent of the geometry of the features, the switching current density obtained for all measured constrictions should be roughly identical, within the bounds of experimental fluctuations. That is what is observed in figure 40 when plotting the switching current density obtained from constrictions NWE 0.25 and NWE 0.5 together. NWE 2.5 gave a similar behaviour at high temperatures but diverged to higher switching current density at temperatures below 15 K.

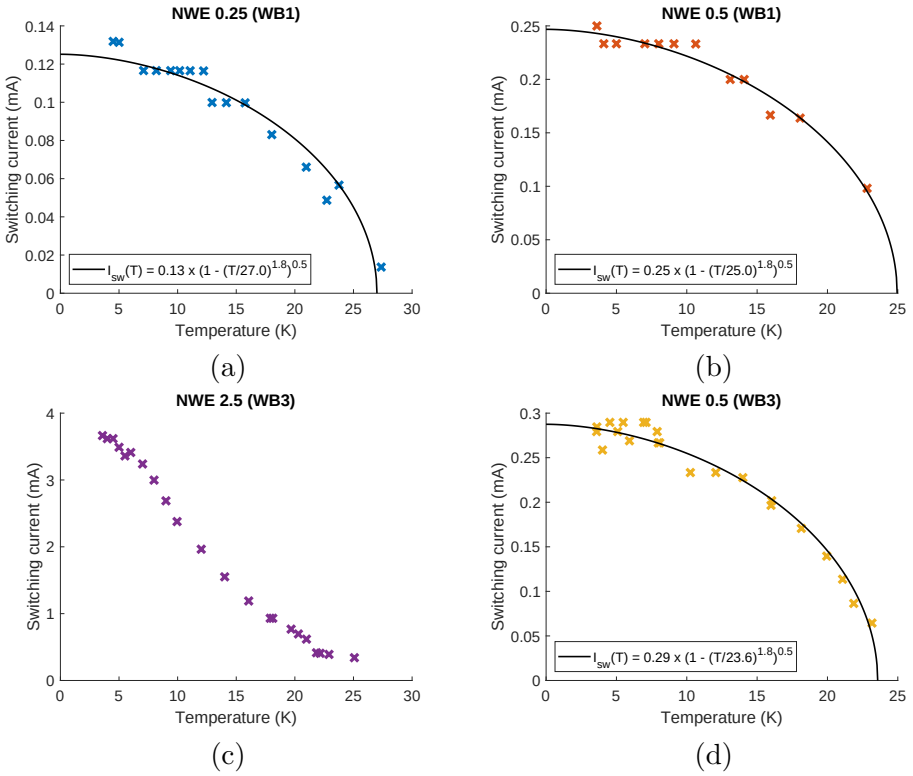


Figure 39: Switching current vs temperature of several constrictions of width (a) 0.25 µm, (b) 0.5 µm, (c) 0.5 µm, (d) 2.5 µm, extracted from their IV curves.

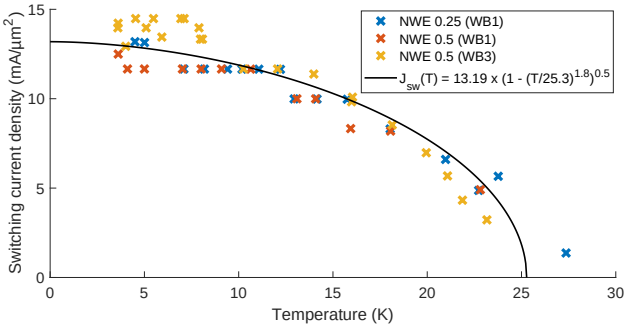


Figure 40: Switching current density vs temperature of several constrictions of width $0.25\mu m$ (blue), $0.5\mu m$ (orange), $0.5\mu m$ (yellow), extracted from their IV curves.

The switching current density to temperature equation fitted suggests that the film critical temperature is around 25.3 K and its critical switching current density is around 13.19 mA µm^{-2}. This result is not the same as the one obtained from the first measurements in the probe-station (see section 4.3.1, we found $J_s w(9\,\mathrm{K}) \approx 22\,\mathrm{mA\,\mu m^{-2}}$), even if they remain in the same order of magnitude. The main comment that can be made here is that those experiments are not very robust; for example, the temperature sweeps are performed only once and the temperature set manually. In the next section, we will focus on properly measuring the switching current distributions and try to extract with exactitude physical properties of the devices and material.

4.4 Switching current characterization

4.4.1 Setup and measurements

The setup used to perform the measurements is schematized in figure 41. An Arbitrary Waveform Generator (AWG) is used to repeatedly send a ramp current (ramp voltage transformed by adding a series resistor R_S) through the device. As previously, the devices are wire-bonded to a PCB and cooled down in the freespace; see section 4.3.2 for more details. The output current is sent to an oscilloscope for analysis and recording. The oscilloscope also records a square signal from the AWG, synchronized with the ramp signal, acting like a clock for the measurements.

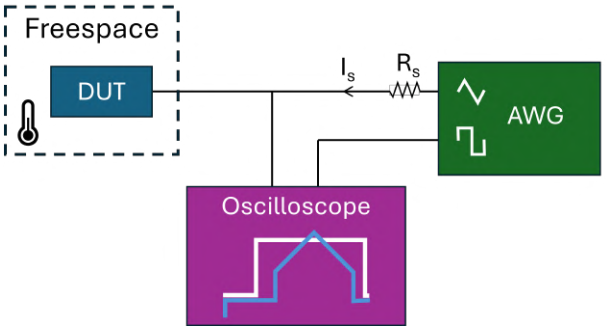


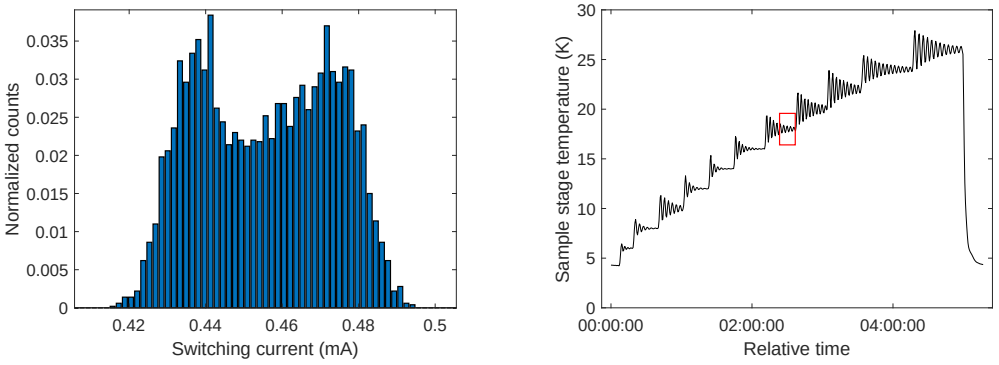
Figure 41: Electrical diagram of the setup for obtaining switching current histograms of devices at various temperatures in the freespace. *Note that the lines represent BNC cables.*

The scope is first manually set by adjusting the trigger and skew settings. Then, for each temperature, the following automated steps are performed:

1. Set the temperature and wait for its stabilization.
2. Set the AWG to ramp up the signal to the indicated maximum current $\hat{I}_S$ at the frequency f, i.e with a ramping rate $\frac{dI}{dt} = \hat{I}_S \times 4f$.
3. Set the scope to measure and record, for a given number of triggers, the switching time Δt distribution.
4. Set the AWG and the oscilloscope back to idle.
5. Save the data recorded by the oscilloscope.
6. Repeat the steps for the next temperature.

The freespace system includes heaters on the sample stage and a temperature sensor located on the 3K stage for closed-loop control. The PID settings for the heaters were not initially optimized and required tuning. Although there is room for further improvement, we were able to achieve and stabilize at almost any temperature within a maximum of 20 minutes, regardless of the temperature jump amplitude, whereas previously it could take more than an hour at high temperatures. Indeed, the temperature sensor itself has a response time dependant on the temperature.

Maintaining a stable temperature was crucial as it influenced the shape of the switching current histograms. This is illustrated in figure 42, which shows a double-Gaussian shaped histogram obtained for a constriction when the temperature was oscillating during the measurement (5000 sweeps sweeps recorded in approximately 710 s). It provides an example of a measurement taken before the PID was properly optimized. The red rectangle in (b) highlights the moment when the histogram in (a) was recorded.



(a) (b)

Figure 42: (a) Example of a histogram obtained when the temperature is poorly stabilized. (b) The temperature profile of such measurement. The red frame is the time during which the histogram was recorded.

Another crucial measurement setup to discuss is how the switching delay Δt is defined (found) by the oscilloscope. Figure 43 schematizes the output signal received by the oscilloscope from which the switching time needs to be extracted. In the measurements, we selected the delay before the switching event to be the positive skew between:

1. the clock rise at 50 % of its signal amplitude and
2. the output current deskew exceeding an absolute threshold selected to be as close as possible to the signal noise.

The hysteresis of the signals triggers for the skew settings were also optimally set to avoid false counts.

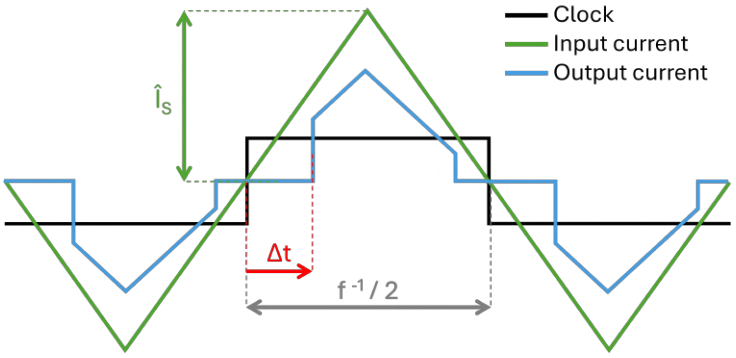


Figure 43: Schematic of the signals amplitude in time, used for measuring the switching current distribution.

After the data in switching delay Δt is saved, it can be translated to a switching current I_{sw} by the following relation:

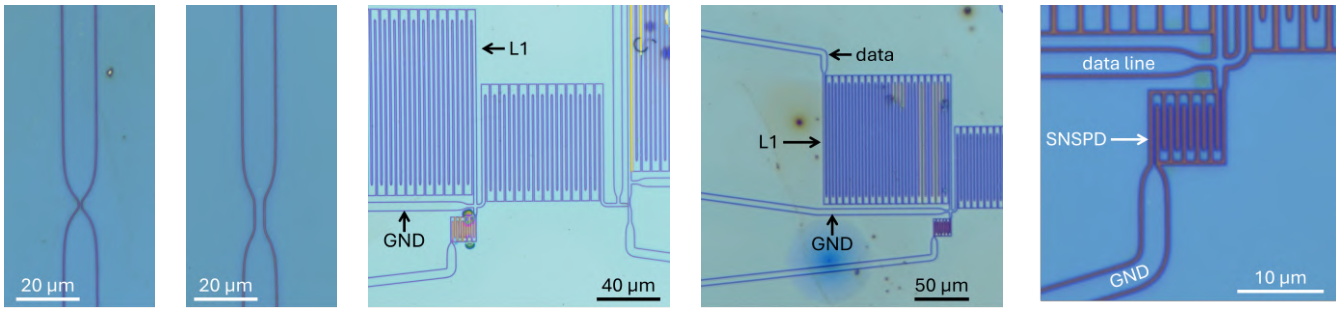
$$\frac{\Delta t}{f^{-1}/4} = \frac{I_{sw}}{\hat{I}_S} \tag{4}$$

The data recorded for several devices is summarized in table 2. Two constrictions and 3 meanders were tested following the procedure described in section 4.4.1. Note that after the fabrication run, only a few devices were suitable for testing, and some adjustments were made to probe them. Specifically, meanders C and D were originally designed to be inductors for a larger circuit. The ground was relocated as shown in Figure 44(c and d), and the other lines

were left open. Similar adjustments were made to probe nanowire E, as illustrated in Figure 44(e).

ID		ID on chip	type	width	length
A		NWE 0.5 + shunt	constriction	0.5 µm	-
B		NWE 2.5	constriction	2.5 µm	-
C		SNSPD-NTRON-01-B L1 + shunt	meander	1.5 µm	4.3 mm
D		SNSPD-NTRON-01-C L1	meander	1.5 µm	4.3 mm
E		SNSPD-NTRON-005-C SNSPD	meander	0.25 µm	70 µm

Table 2: Nanowires tested and presented in this section.



(a) (b) (c) (d) (e)

Figure 44: Optical images of the nanowires tested. (a) A 0.5 µm, (b) B 2.5 µm, (c) C 1.5 µm, (d) D 1.5 µm and (e) E 0.25 µm.

First of all, the typical data obtained after running one measurement is given in figure 45. It contains N histograms for N temperatures of recording. Not surprisingly, the histograms appear to shift to lower currents when the temperature increases.

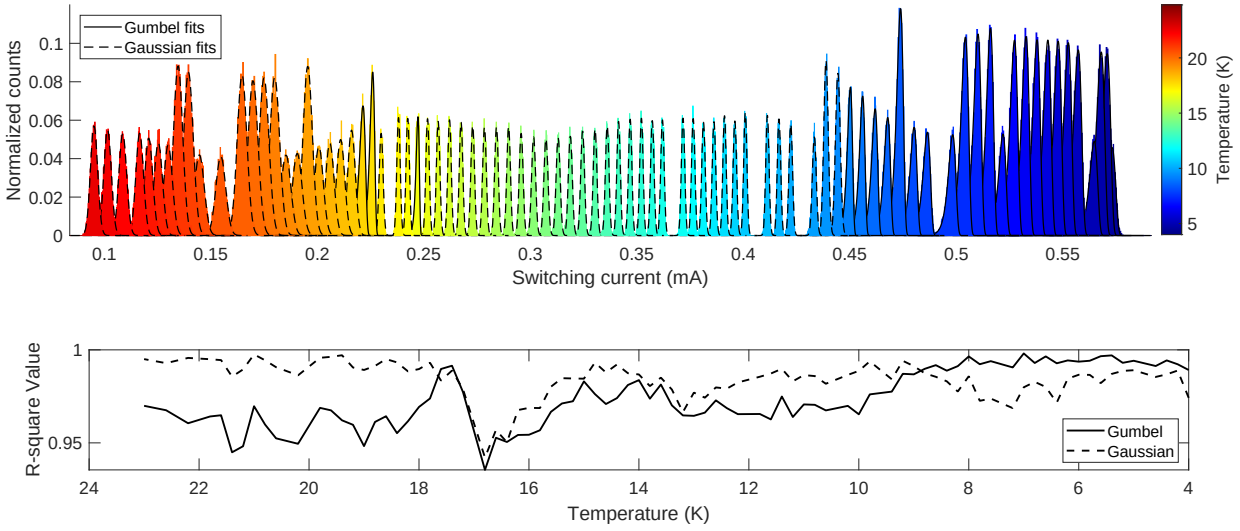
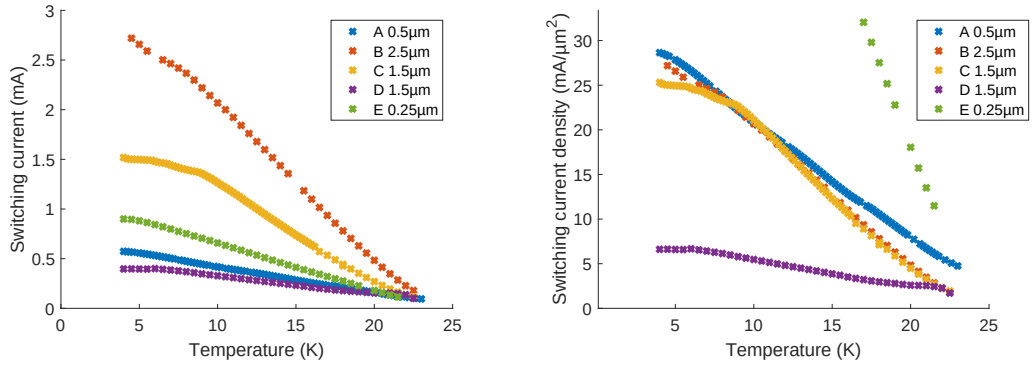


Figure 45: (top) Switching current distributions measured on nanowire A ('NWE 0.5 + shunt') at temperatures ranging from 4K to 23K. (bottom) Corresponding goodness of fit (r-square value) for Gumbel and Gaussian distributions over the temperature range of the measurement.

4.4.2 Results and discussion

From all switching currents recorded, we can plot the mean switching current, and the mean switching current density, versus temperature and we obtain the graphs displayed in figure 46. We observe that devices A, B and C have relatively similar switching current densities distribution over temperature whereas devices D and E are completely out. This observation constitutes a good evidence for the fact that the superconducting (MgB_2) layer was not affected evenly during the fabrication.

When looking at device D, supposed to be identical to C, we also observe that it switches earlier than expected: its critical current is below 0.5 mA instead of 1.5 mA for the similar meander C. A discrepancy in the patterned meander could be the reason for this difference, causing the nanowire to switch earlier, always at the same point on the current path. This mention highlights the importance of round shapes and optimal steps in the layout's design, to prevent edges and sharp angles to be responsible for the limiting current instead of the designed nanowire. To conclude this parenthesis, when aiming to extract physical properties of a superconducting material through the analysis of nanowire switching current distributions, it is preferable to use simple geometries (such as simple constrictions) for the nanowires. This approach ensures high confidence in the switching region and allows for accurate data collection.



(a) (b)

Figure 46: Switching current (a) and switching current density (b) vs temperature of several nanowires, extracted from their histograms.

Before extracting any further parameters from these measurements, we need to discuss the validity of the collected data. When analyzing the goodness of fit for Gaussian and Gumbel distributions, whose probability density functions are given in equations 5 and 6 respectively, we observed that most nanowires tested fit better with a Gaussian distribution at higher temperatures and a Gumbel distribution at lower temperatures (see figure 45). This was unexpected, as we anticipated all fits to follow a Gumbel distribution. [14]

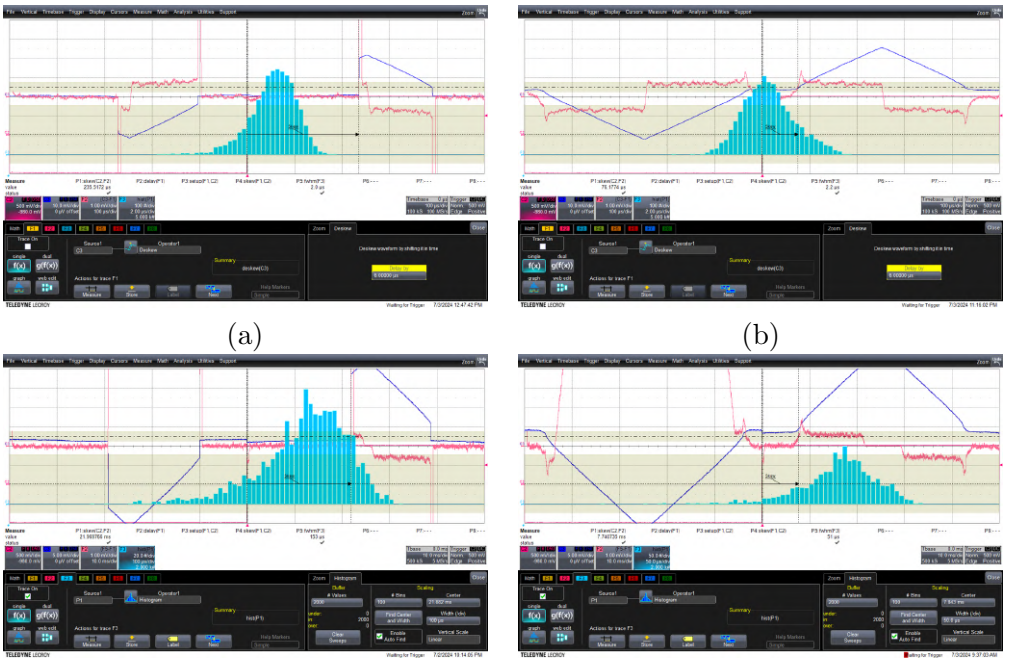
$$f(x) = \frac{1}{\sqrt{2\pi\sigma^2}} \exp\left(-\frac{(x-\mu)^2}{2\sigma^2}\right) \tag{5}$$

$$f(x) = \frac{1}{\beta} \exp\left(-\left(\frac{x-\mu}{\beta}\right) - \exp\left(-\frac{x-\mu}{\beta}\right)\right) \tag{6}$$

New measurements were conducted where oscilloscope screenshots were taken at each temperature. At high temperatures, we observed no jump in the output current during the transition from superconducting to resistive. This difference could be a physical phenomena, it could as well be due to a low signal-to-noise ratio. After repeating one measurement at 10 Hz instead

of 1 kHz, we could still see this shape in the signal, allowing us to conclude that this issue is independent from the frequency of the input current.

Figure 47 gives screenshots of the oscilloscope screen for the two different frequencies at low and high temperature. The change at high temperature of the output current (blue curve) shape is clear and in such cases the notion of switching is not well defined. In any case, the mean switching currents derived from these "jump-less" signals are still accurate. On the contrary, we cannot strongly affirm that the distribution shapes, and hence their standard deviation and switching rates, are accurate as well.



(a) (b) (c) (d)

Figure 47: Screenshots of the oscilloscope during measurement at 1 kHz (top) and 10 Hz (bottom) at low (left) and high (right) temperature: (a) 4K, (b) 19K, (c) 5.5K, (d) 18.5K. The blue channel is the output current sensed from the DUT. The pink squared signal is the clock sent from the AWG. The other pink channel is the channel used for recording the switching events, displayed in the histogram in blue. The screenshots concern measurements taken on nanowire 'A 0.5 µm'

Another question related to the accuracy of acquired data was asked: is there any correlated oscillation in time of the raw switching currents measured for each histogram. Indeed, the collected histograms do not provide the information in time/sequence. The raw data was recorded in sequence over 10000 measurements of switching delay for the nanowire E, at 4 K. It is given in figure 48 in a time domain next to its equivalent Fourier transform, revealing a single significant peak at 0 frequency, corresponding to the signal's offset. Consequently, we consider the measurements to be fast enough for the histograms not to be affected by fluctuations in the setup or freespace.

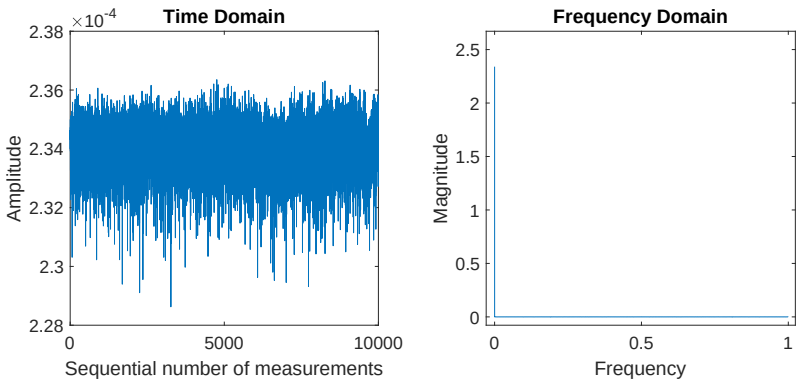


Figure 48: 10000 recordings of switching delays measured by the oscilloscope on nanowire E at 4 K plotted in a time domain (left) and in its equivalent frequency domain (right) after performing the signal's Fourier transform.

Going back to the switching current distribution analysis streamline, the standard deviations can be plotted with respect to the temperature, as given in figure 49. Distinctive regions can be observed from the plots: a plateau region at low temperature, a jump and a soft decrease as the temperature increases. Although we cannot affirm with certainty that the observed phenomena have a real physical explanation, this behaviour is still worth noting, and might be explained with further testing.

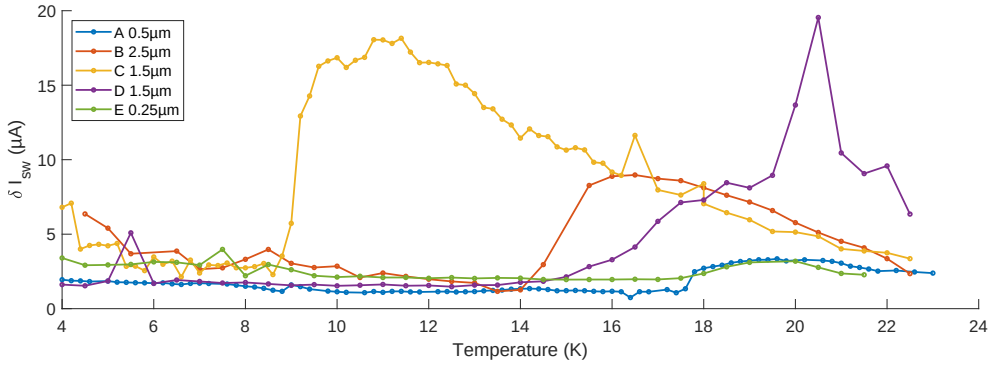
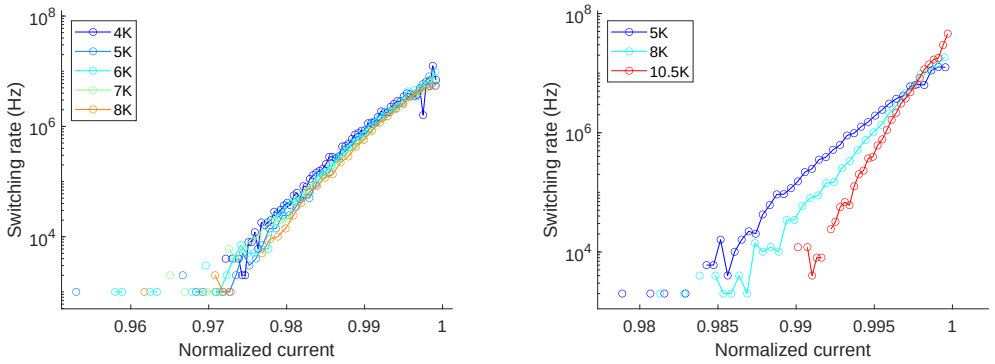


Figure 49: Switching current standard deviation versus temperature of histograms obtained from the measured nanowires.

Furthermore, the switching rates can be directly extracted from the histograms after applying the Kurkijärvi-Fulton-Dunkleberger transformation [8], following equation 7. $\frac{dI}{dt}$ is the current sweep rate, ΔI the current bin width and $P(i)$ the number of counts in the channel i.

$$\Gamma_{sw} = \frac{dI}{dt}\frac{1}{\Delta I} \ln\left(\sum_{j=1}^{K} P(j) / \sum_{i=1}^{K-1} P(i)\right) \tag{7}$$

It gives more physical meaning behind our simple measurements as the switching rate represents as well the measured dark-count rate and the fluctuation-event rate [21]. Figure 50 gives the switching rates obtained from selected histograms/temperatures of the two constrictions (A and B).



(a) (b)

Figure 50: Switching rates versus normalized bias current for different temperatures of nanowires (a) A 0.5 µm and (b) B 2.5 µm.

4.5 Outlook of the devices characterization

A fair amount of measurements were performed on the chip, despite the non perfect fabrication run. Work is still to be completed in order to fit theoretical models to the acquired data, based on nanowires dimensions considerations, particularly regarding the analysis of the switching current distribution. Note that we coded and implemented theoretical models to be fitted to our data, but were not able to reach a conclusion due to the lack of knowledge on Magnesium Diboride material properties. Quantities such as the electron diffusivity, the specific heat or the charge imbalance time of MgB_2 were unknown. [14] Generally speaking, figuring out theoretical models for MgB_2 is the work of physicists and material scientists.

Furthermore, the lack of a good definition of the switching event at high temperature when triggering on the voltage across the nanowire is an concern that needs to be addressed. Is this shape expected at such temperature, or can it be corrected by increasing the signal to noise ration in the setup, for example by adding Low Noise Amplifier at the output of the device under test?

Other small improvements can be implemented such as including a ground plane in the pads layer of the GDS file for facilitating probing, better remotely controlling the oscilloscope settings for histograms recordings, or even further tuning the freespace PID.

5 Conclusion

The main takeaway results of this work are as follows. First, we successfully defined and implemented a solid structure for designing GDS files for the fabrication of commonly used nanowire electronics devices and circuits into a Python-based tool. We believe that qnngds could become the foundation for any nanowire electronics fabrication design if contributions are frequent and rigorously follow the proposed design workflow and library organization.

Second, we proposed a new process flow for fabricating devices in MgB_2 using samples provided by the Jet Propulsion Laboratory. Although the process requires significant refinements, we managed to fabricate nanowires with widths down to 0.25 µm that exhibit superconductivity up to a critical temperature of around 24 K.

Furthermore, we have paved the way for future studies within the group by analyzing switching current distributions. This analysis aims to investigate the physical mechanisms responsible for fluctuation phenomena and the overcoming of the energy barrier associated with switching events in nanowires.

Looking ahead, we will discuss the next steps of the project and outline the future directions for the design, fabrication and characterization aspects of the project. On the design part, the Python package is operational and ready to be used. However, its library is still very limited, and many improvements are needed. The feedback and contributions from each new user are the main outlook expected for this work. A list of issues to help improve the tool and report bugs is accessible on the GitHub page of the project.

On the fabrication part of the project, a second run was performed after learning from the first one: a different e-beam resist was used, the hard mask was made of SiN instead of SiO_2, etch recipes were adjusted, and other layout considerations such as avoiding sharp angles around nTrons gate or spreading the ground to enable GDG-probing were made. The ultimate goal of the fabrication is to maximize control over the etching steps in terms of etch rates, selectivity, and pattern transfer with high fidelity, all while minimizing the alteration of the material properties surrounding the etching.

Finally, on the measurement of the switching current distributions, the main improvements to focus on are making the output signal more readable at high temperatures (for example, by adding an LNA to the setup), improving remote control of the oscilloscope to fine-tune its measurements according to the temperature, and determining specific material properties of Magnesium Diboride to compare models and acquired data.

From a personal point of view, I have learned a lot. Building the Python package strengthened my coding skills and understanding of this domain. Even though I was already familiar with generating layouts with code, I learned to use Phidl, which focuses on nanoscale designing. I was not familiar with any nanoscale fabrication aspects and learned about the challenges of e-beam lithography: the design constraints brought by exposure time and cost, the preparation of the exposure work including beam corrections, and the exposure process itself were all new to me. Despite not being a direct cleanroom operator on the machines, I observed the functioning of a different facility than the CMi at EPFL and certainly learned from it as well. Wire-bonding was also new to me, and hours of practice and perseverance have now made me proficient. Experimentally speaking, I had the chance to work on state-of-the-art machines like the Lake Shore probe-station and the freespace cryostat. I also discovered the power of automated measurements and remotely controlling equipment, which I had never used before. Finally, I had little to no background in the theory of superconductivity and significantly benefited from the weekly journal clubs as well as the sharing of other students' work at the superconductivity team meetings.

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Appendix

Run	ID	Gate		Drain	
		Width	Status	Width	Status
(1)	ntronA	0.25 µm	open	2.5 µm	shorted
(2)	ntronB	0.1 µm	open	2.0 µm	SC
(2)	ntronB	0.25 µm	open	1.25 µm	SC
(3)	ntronA	0.5 µm	shorted	10.0 µm	shorted
(3)	ntronC	0.25 µm	shorted	2.5 µm	SC

Table 3: Ntrons tested in the freespace. Statuses of their gate and channel are given. All gates were open.

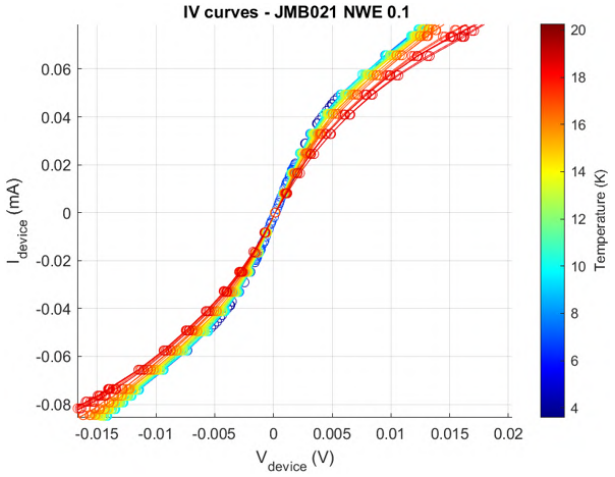

Figure 51: IV curve of a constriction of supposed width of 0.1 µm at temperatures from 4K to 30K. We observe that this constriction is resistive and not superconducting.